

# Supply Voltage Supervisor

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This chapter describes the operation of the SVS. The SVS is implemented in MSP430x15x and MSP430x16x devices.

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## 6.1 SVS Introduction

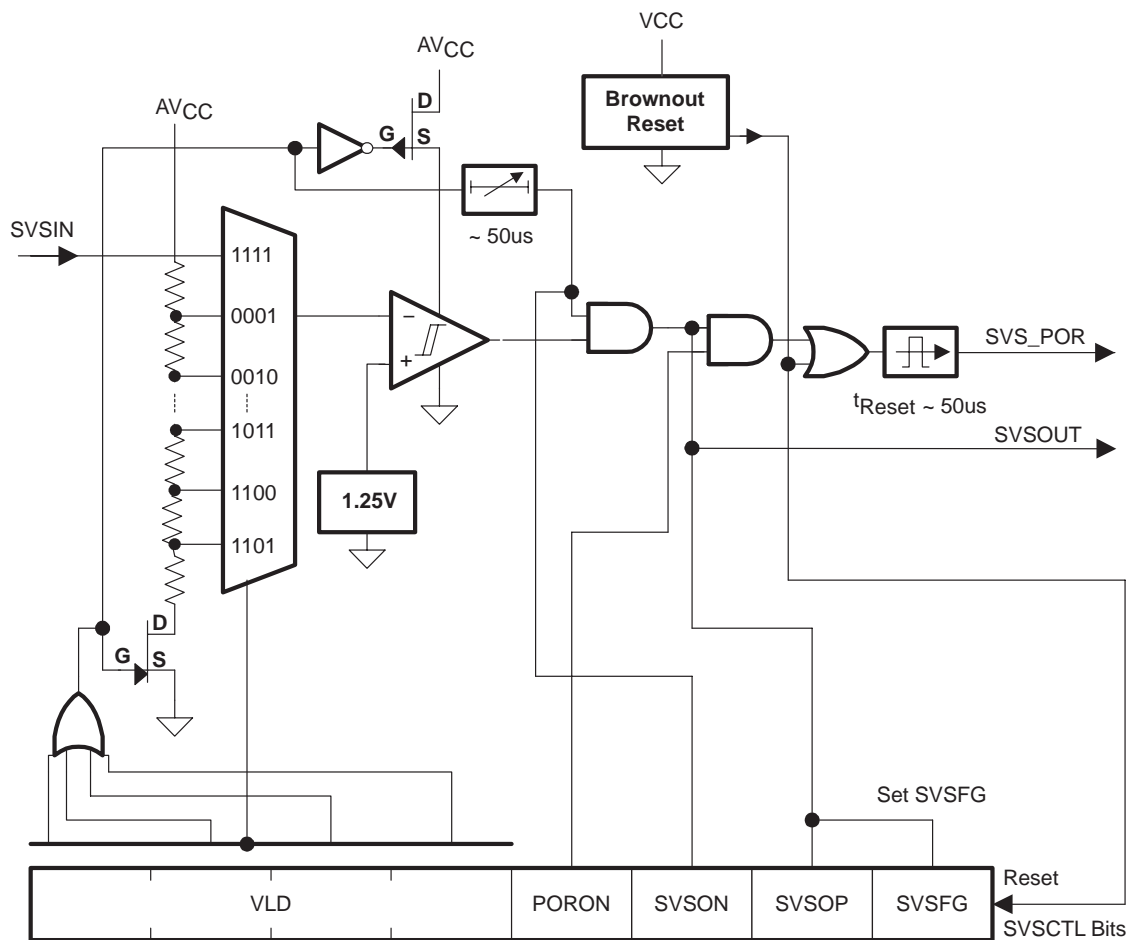
The supply voltage supervisor (SVS) is used to monitor the  $AV_{CC}$  supply voltage or an external voltage. The SVS can be configured to set a flag or generate a POR reset when the supply voltage or external voltage drops below a user-selected threshold.

The SVS features include:

- ☐  $AV_{CC}$  monitoring
- ☐ Selectable generation of POR
- ☐ Output of SVS comparator accessible by software
- ☐ Low-voltage condition latched and accessible by software
- ☐ 14 selectable threshold levels
- ☐ External channel to monitor external voltage

The SVS block diagram is shown in Figure 6–1.

Figure 6–1. SVS Block Diagram



## 6.2 SVS Operation

The SVS detects if the  $AV_{CC}$  voltage drops below a selectable level. It can be configured to provide a POR or set a flag, when a low-voltage condition occurs. The SVS is disabled after a brownout reset to conserve current consumption.

### 6.2.1 Configuring the SVS

The  $VLDx$  bits are used to enable/disable the SVS and select one of 14 threshold levels ( $V_{(SVS\_IT-)}$ ) for comparison with  $AV_{CC}$ . The SVS is off when  $VLDx = 0$  and on when  $VLDx > 0$ . The  $SVSON$  bit does not turn on the SVS. Instead, it reflects the on/off state of the SVS and can be used to determine when the SVS is on.

When  $VLDx = 1111$ , the external  $SVSIN$  channel is selected. The voltage on  $SVSIN$  is compared to an internal level of approximately 1.2 V.

### 6.2.2 SVS Comparator Operation

A low-voltage condition exists when  $AV_{CC}$  drops below the selected threshold or when the external voltage drops below its 1.2-V threshold. Any low-voltage condition sets the  $SVSFG$  bit.

The  $PORON$  bit enables or disables the device-reset function of the SVS. If  $PORON = 1$ , a POR is generated when  $SVSFG$  is set. If  $PORON = 0$ , a low-voltage condition sets  $SVSFG$ , but does not generate a POR.

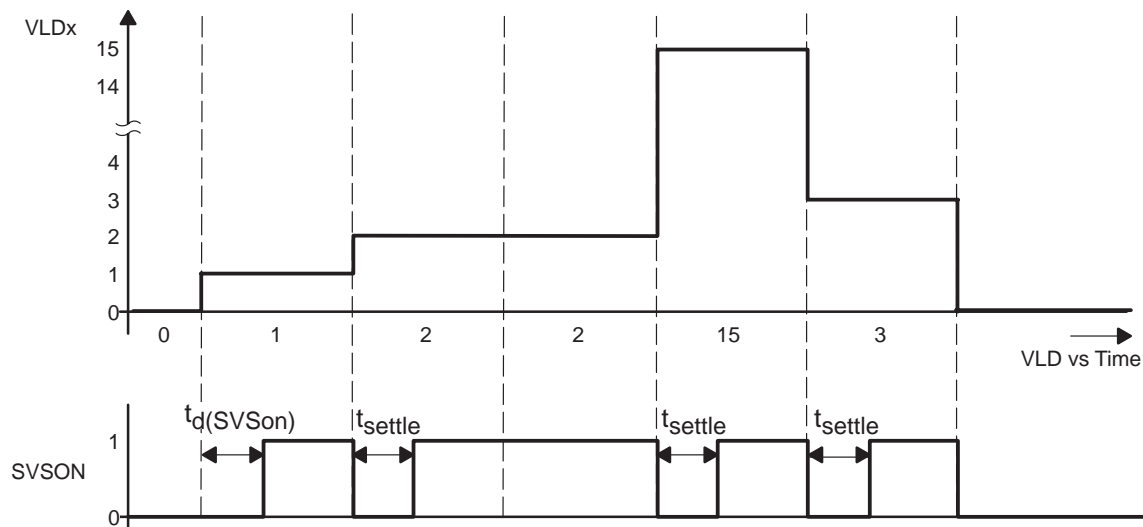
The  $SVSFG$  bit is latched. This allows user software to determine if a low-voltage condition occurred previously. The  $SVSFG$  bit must be reset by user software. If the low-voltage condition is still present when  $SVSFG$  is reset, it will be immediately set again by the SVS.

### 6.2.3 Changing the VLDx Bits

When the VLDx bits are changed, two settling delays are implemented to allow the SVS circuitry to settle. During each delay, the SVS will not set SVSFG. The delays,  $t_d(\text{SVSON})$  and  $t_{\text{settle}}$ , are shown in Figure 6–2. The  $t_d(\text{SVSON})$  delay takes effect when VLDx is changed from zero to any non-zero value and is approximately 50  $\mu\text{s}$ . The  $t_{\text{settle}}$  delay takes effect when the VLDx bits change from any non-zero value to any other non-zero value and is a maximum of ~12  $\mu\text{s}$ . See the device-specific datasheet for the delay parameters.

During the delays, the SVS will not flag a low-voltage condition or reset the device, and the SVSON bit is cleared. Software can test the SVSON bit to determine when the delay has elapsed and the SVS is monitoring the voltage properly.

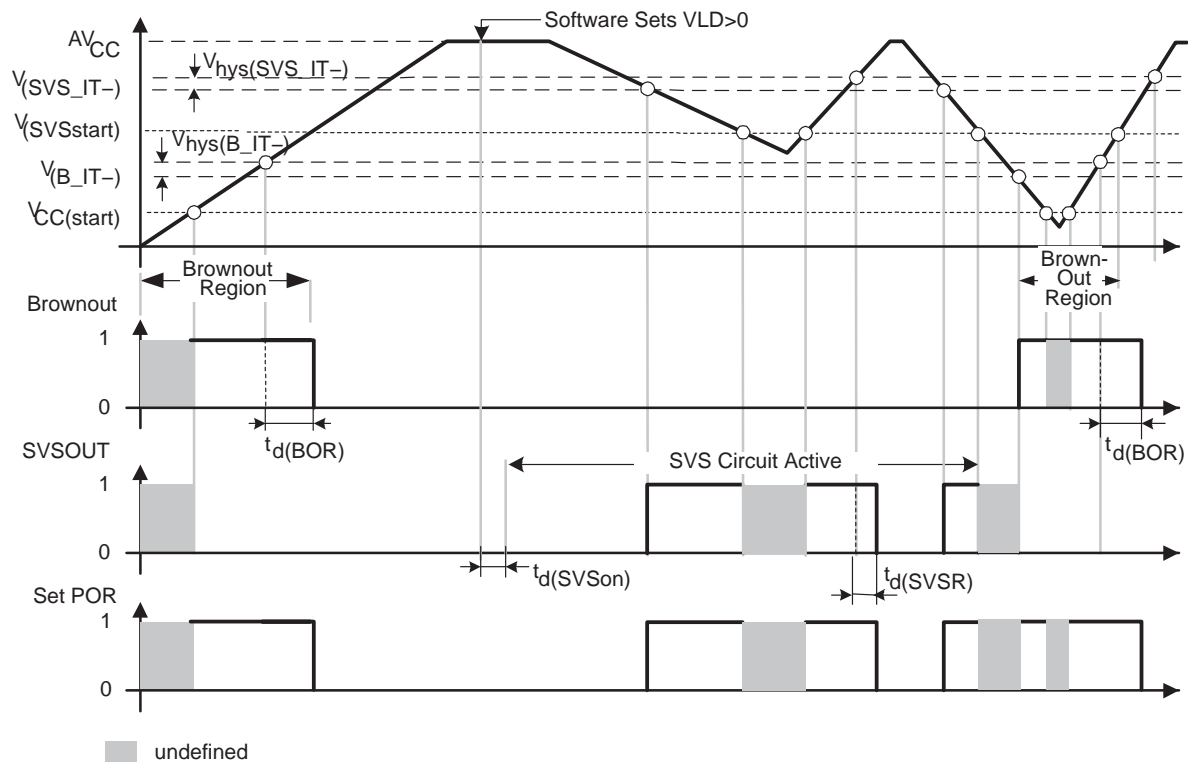
Figure 6–2. SVSON state When Changing VLDx



### 6.2.4 SVS Operating Range

Each SVS level has hysteresis to reduce sensitivity to small supply voltage changes when  $AV_{CC}$  is close to the threshold. The SVS operation and SVS/Brownout interoperation are shown in Figure 6–3.

Figure 6–3. Operating Levels for SVS and Brownout/Reset Circuit



### 6.3 SVS Registers

The SVS registers are listed in Table 6–1.

Table 6–1. SVS Registers

Register	Short Form	Register Type	Address	Initial State
SVS Control Register	SVSCTL	Read/write	055h	Reset with BOR

#### SVSCTL, SVS Control Register

7	6	5	4	3	2	1	0
VLDx				PORON	SVSON	SVSOP	SVSFG
rw-0†	rw-0†	rw-0†	rw-0†	rw-0†	r	r	rw-0†

† Reset by a brownout reset only, not by a POR or PUC.

<b>VLDx</b>	Bits 7-4	<p>Voltage level detect. These bits turn on the SVS and select the nominal SVS threshold voltage level. See the device-specific datasheet for parameters.</p> <p>0000 SVS is off</p> <p>0001 1.9 V</p> <p>0010 2.1 V</p> <p>0011 2.2 V</p> <p>0100 2.3 V</p> <p>0101 2.4 V</p> <p>0110 2.5 V</p> <p>0111 2.65 V</p> <p>1000 2.8 V</p> <p>1001 2.9 V</p> <p>1010 3.05 V</p> <p>1011 3.2 V</p> <p>1100 3.35 V</p> <p>1101 3.5 V</p> <p>1110 3.7 V</p> <p>1111 Compares external input voltage SVSIN to 1.2 V.</p>
<b>PORON</b>	Bit 3	<p>POR on. This bit enables the SVSFG flag to cause a POR device reset.</p> <p>0 SVSFG does not cause a POR</p> <p>1 SVSFG causes a POR</p>
<b>SVSON</b>	Bit 2	<p>SVS on. This bit reflects the status of SVS operation. This bit DOES NOT turn on the SVS. The SVS is turned on by setting VLDx &gt; 0.</p> <p>0 SVS is Off</p> <p>1 SVS is On</p>
<b>SVSOP</b>	Bit 1	<p>SVS output. This bit reflects the output value of the SVS comparator.</p> <p>0 SVS comparator output is low</p> <p>1 SVS comparator output is high</p>
<b>SVSFG</b>	Bit 0	<p>SVS flag. This bit indicates a low voltage condition. SVSFG remains set after a low voltage condition until reset by software or a brownout reset.</p> <p>0 No low voltage condition occurred</p> <p>1 A low condition is present or has occurred</p>