Chapter 9

# Supply Voltage Supervisor (SVS)

This chapter describes the operation of the SVS. The SVS is implemented in selected MSP430x2xx devices.

## 9.1 Supply Voltage Supervisor (SVS) Introduction

The SVS is used to monitor the $AV_{CC}$ supply voltage or an external voltage. The SVS can be configured to set a flag or generate a POR reset when the supply voltage or external voltage drops below a user-selected threshold.

The SVS features include:

- $AV_{CC}$ monitoring
- Selectable generation of POR
- Output of SVS comparator accessible by software
- Low-voltage condition latched and accessible by software
- 14 selectable threshold levels
- External channel to monitor external voltage

The SVS block diagram is shown in Figure 9-1.

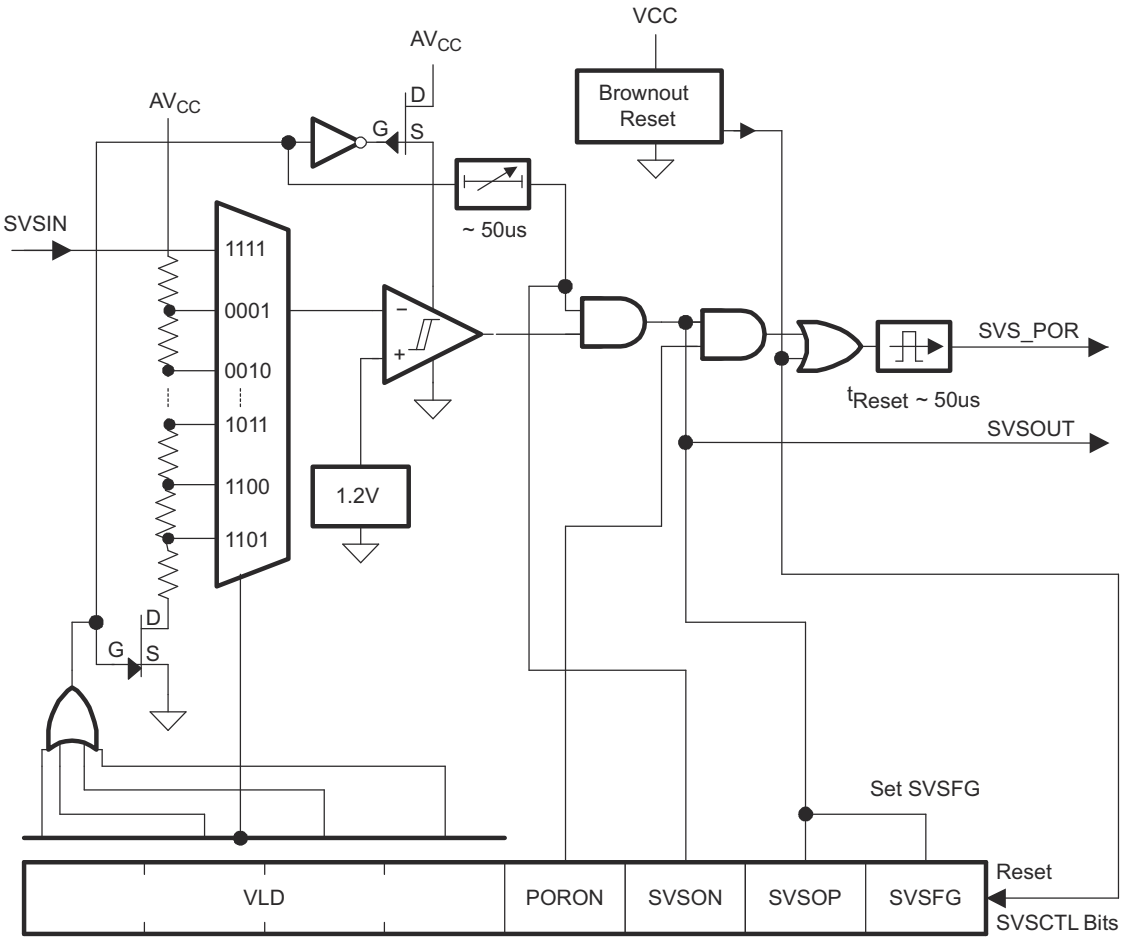


**Figure 9-1. SVS Block Diagram**

## 9.2 SVS Operation

The SVS detects if the $AV_{CC}$ voltage drops below a selectable level. It can be configured to provide a POR or set a flag, when a low-voltage condition occurs. The SVS is disabled after a brownout reset to conserve current consumption.

### 9.2.1 Configuring the SVS

The VLDx bits are used to enable/disable the SVS and select one of 14 threshold levels ($V_{(SVS\_IT-)}$) for comparison with $AV_{CC}$. The SVS is off when VLDx = 0 and on when VLDx > 0. The SVSON bit does not turn on the SVS. Instead, it reflects the on/off state of the SVS and can be used to determine when the SVS is on.

When VLDx = 1111, the external SVSIN channel is selected. The voltage on SVSIN is compared to an internal level of approximately 1.25 V.

### 9.2.2 SVS Comparator Operation

A low-voltage condition exists when $AV_{CC}$ drops below the selected threshold or when the external voltage drops below its 1.25-V threshold. Any low-voltage condition sets the SVSFG bit.

The PORON bit enables or disables the device-reset function of the SVS. If PORON = 1, a POR is generated when SVSFG is set. If PORON = 0, a low-voltage condition sets SVSFG, but does not generate a POR.

The SVSFG bit is latched. This allows user software to determine if a low-voltage condition occurred previously. The SVSFG bit must be reset by user software. If the low-voltage condition is still present when SVSFG is reset, it will be immediately set again by the SVS.

### 9.2.3 Changing the VLDx Bits

When the VLDx bits are changed from zero to any non-zero value there is a automatic settling delay $t_{d(SVSon)}$ implemented that allows the SVS circuitry to settle. The $t_{d(SVSon)}$ delay is approximately 50 µs. During this delay, the SVS will not flag a low-voltage condition or reset the device, and the SVSON bit is cleared. Software can test the SVSON bit to determine when the delay has elapsed and the SVS is monitoring the voltage properly. Writing to SVSCTL while SVSON = 0 will abort the SVS automatic settling delay, $t_{d(SVSon)}$, and switch the SVS to active mode immediately. In doing so, the SVS circuitry might not be settled, resulting in unpredictable behavior.

When the VLDx bits are changed from any non-zero value to any other non-zero value the circuitry requires the time $t_{settle}$ to settle. The settling time $t_{settle}$ is a maximum of ~12 µs. See the device-specific data sheet. There is no automatic delay implemented that prevents SVSFG to be set or to prevent a reset of the device. The recommended flow to switch between levels is shown in the following code.

```
; Enable SVS for the first time:
   MOV.B   #080h,&SVSCTL   ; Level 2.8V, do not cause POR
                           ; ...
; Change SVS level
   MOV.B   #000h,&SVSCTL   ; Temporarily disable SVS
   MOV.B   #018h,&SVSCTL   ; Level 1.9V, cause POR
                           ; ...
```

### 9.2.4 SVS Operating Range

Each SVS level has hysteresis to reduce sensitivity to small supply voltage changes when $AV_{CC}$ is close to the threshold. The SVS operation and SVS/Brownout interoperation are shown in Figure 9-2.

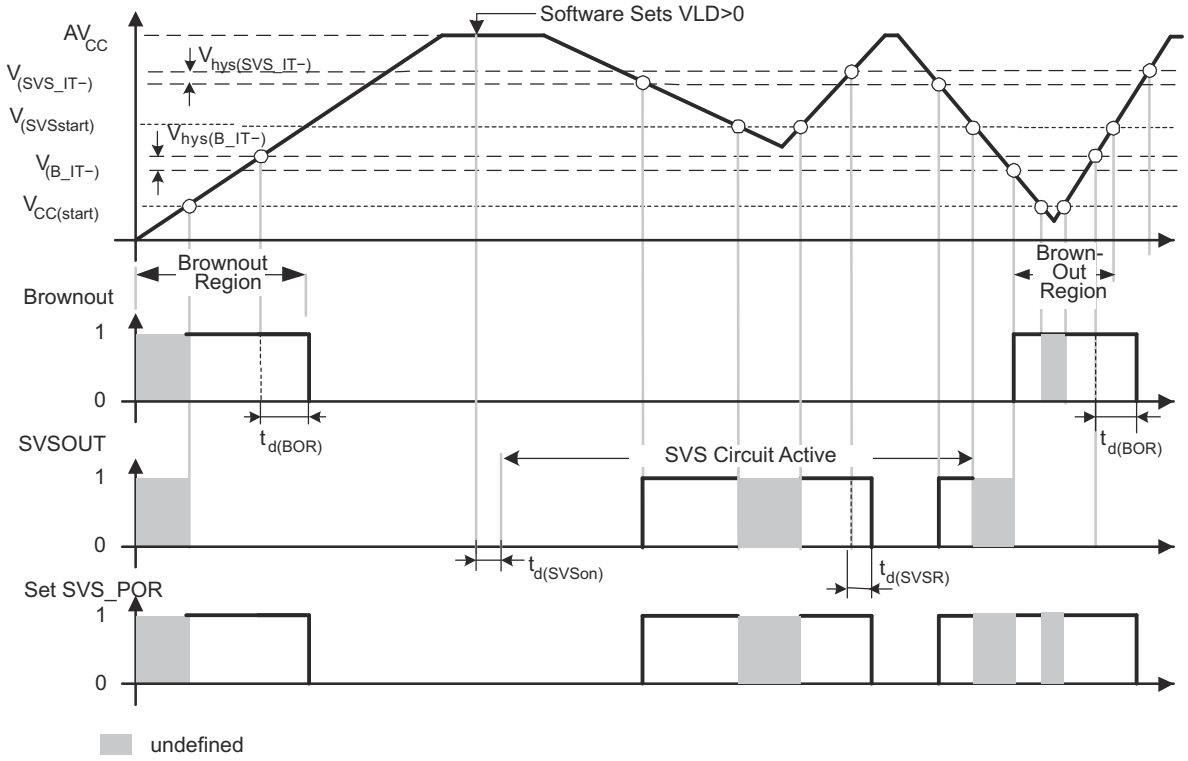


**Figure 9-2. Operating Levels for SVS and Brownout/Reset Circuit**

## 9.3 SVS Registers

Table 9-1 lists the memory-mapped registers for the SVS.

**Table 9-1. SVS Registers**

| Address | Acronym | Register Name | Type | Reset | Section |
|---|---|---|---|---|---|
| 55h | SVSCTL | SVS control | Read/write | 00h with BOR | Section 9.3.1 |

### 9.3.1 SVSCTL Register

SVS Control Register

SVSCTL is shown in Figure 9-3 and described in Table 9-2.

Return to Table 9-1.

**Figure 9-3. SVSCTL Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VLDx | | | | PORON | SVSON | SVSOP | SVSFG |
| rw-0 (1) | rw-0 (1) | rw-0 (1) | rw-0 (1) | rw-0 (1) | r-0 (1) | r-0 (1) | rw-0 (1) |

**Table 9-2. SVSCTL Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | VLDx | R/W | 0h(1) | Voltage level detect. These bits turn on the SVS and select the nominal SVS threshold voltage level. See the device-specific data sheet for parameters.<br>0000b = SVS is off<br>0001b = 1.9 V<br>0010b = 2.1 V<br>0011b = 2.2 V<br>0100b = 2.3 V<br>0101b = 2.4 V<br>0110b = 2.5 V<br>0111b = 2.65 V<br>1000b = 2.8 V<br>1001b = 2.9 V<br>1010b = 3.05 V<br>1011b = 3.2 V<br>1100b = 3.35 V<br>1101b = 3.5 V<br>1110b = 3.7 V<br>1111b = Compares external input voltage SVSIN to 1.25 V |
| 3 | PORON | R/W | 0h(1) | POR on. This bit enables the SVSFG flag to cause a POR device reset.<br>0b = SVSFG does not cause a POR<br>1b = SVSFG causes a POR |
| 2 | SVSON | R | 0h(1) | SVS on. This bit reports the status of SVS operation. This bit DOES NOT turn on the SVS. The SVS is turned on by setting VLDx > 0.<br>0b = SVS is off<br>1b = SVS is on |
| 1 | SVSOP | R | 0h(1) | SVS output. This bit reflects the output value of the SVS comparator.<br>0b = SVS comparator output is low<br>1b = SVS comparator output is high |
| 0 | SVSFG | R/W | 0h(1) | SVS flag. This bit indicates a low-voltage condition. SVSFG remains set after a low-voltage condition until reset by software.<br>0b = No low-voltage condition occurred<br>1b = A low-voltage condition is present or has occurred |

(1) Reset by a brownout reset only, not by a POR or PUC.