



# Power Management Module and Supply Voltage Supervisor

This chapter describes the operation of the Power Management Module (PMM) and Supply Voltage Supervisor (SVS).

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## 2.1 Power Management Module (PMM) Introduction

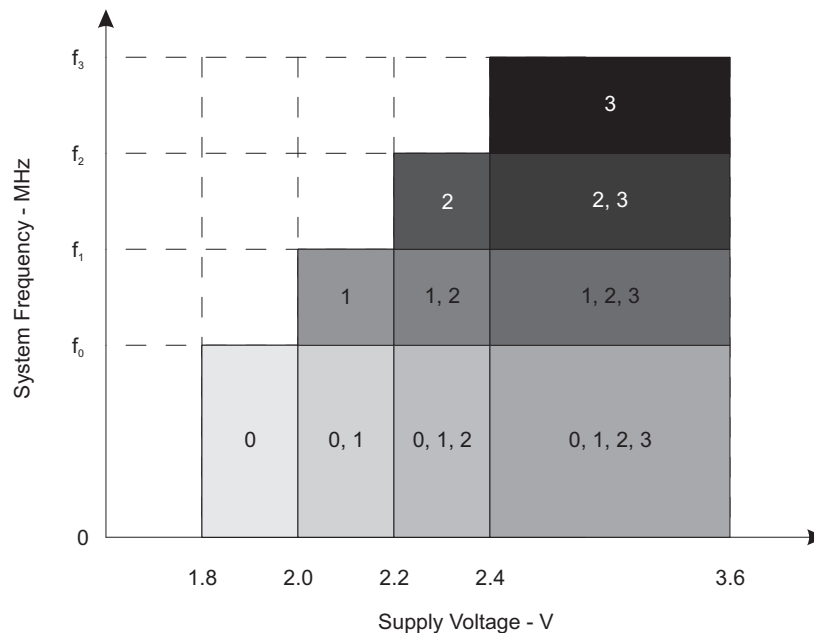
PMM features include:

- Wide supply voltage ( $DV_{CC}$ ) range: 1.8 V to 3.6 V
- Generation of voltage for the device core ( $V_{CORE}$ ) with up to four programmable levels
- Supply voltage supervisor (SVS) for  $DV_{CC}$  and  $V_{CORE}$  with programmable threshold levels
- Supply voltage monitor (SVM) for  $DV_{CC}$  and  $V_{CORE}$  with programmable threshold levels
- Brownout reset (BOR)
- Software accessible power-fail indicators
- I/O protection during power-fail condition
- Software selectable supervisor or monitor state output (optional)

The PMM manages all functions related to the power supply and its supervision for the device. Its primary functions are first to generate a supply voltage for the core logic, and second, provide several mechanisms for the supervision and monitoring of both the voltage applied to the device ( $DV_{CC}$ ) and the voltage generated for the core ( $V_{CORE}$ ).

The PMM uses an integrated low-dropout voltage regulator (LDO) to produce a secondary core voltage ( $V_{CORE}$ ) from the primary one applied to the device ( $DV_{CC}$ ). In general,  $V_{CORE}$  supplies the CPU, memories (flash and RAM), and the digital modules, while  $DV_{CC}$  supplies the I/Os and all analog modules (including the oscillators). The  $V_{CORE}$  output is maintained using a dedicated voltage reference.  $V_{CORE}$  is programmable up to four steps, to provide only as much power as is needed for the speed that has been selected for the CPU. This enhances power efficiency of the system. The input or primary side of the regulator is referred to in this chapter as its high side. The output or secondary side is referred to in this chapter as its low side.

The required minimum voltage for the core depends on the selected MCLK rate. Figure 2-1 shows the relationship between the system frequency for a given core voltage setting, as well as the minimum required voltage applied to the device. Figure 2-1 is only an example—see the device-specific data sheet to determine which core voltage levels are supported and what level of system frequency performance is possible for a given device.



**Figure 2-1. System Frequency, Supply Voltage, and Core Voltage – See Device-Specific Data Sheet**

The PMM module provides means for  $DV_{CC}$  and  $V_{CORE}$  to be supervised and monitored. Both of these functions detect when a voltage falls under a specific threshold. In general, the difference is that supervision results in a power-on reset (POR) event, while monitoring results in the generation of an interrupt flag that software may then handle. As such,  $DV_{CC}$  is supervised and monitored by the high-side supervisor (SVS<sub>H</sub>) and high-side monitor (SVM<sub>H</sub>), respectively.  $V_{CORE}$  is supervised and monitored by the low-side supervisor (SVS<sub>L</sub>) and low-side monitor (SVM<sub>L</sub>), respectively. Thus, there are four separate supervision and monitoring modules that can be active at any given time. The thresholds enforced by these modules are derived from the same voltage reference used by the regulator to generate  $V_{CORE}$ .

In addition to the SVS<sub>H</sub>, SVM<sub>H</sub>, SVS<sub>L</sub>, and SVM<sub>L</sub> modules,  $V_{CORE}$  is further monitored by the brownout reset (BOR) circuit. As  $DV_{CC}$  ramps up from 0 V at power up, the BOR keeps the device in reset until  $V_{CORE}$  is at a sufficient level for operation at the default MCLK rate and for the SVS<sub>H</sub> and SVS<sub>L</sub> mechanisms to be activated. During operation, the BOR also generates a reset if  $V_{CORE}$  falls below a preset threshold. BOR can be used to provide an even lower-power means of monitoring the supply rail if the flexibility of the SVS<sub>L</sub> is not required.

The block diagram of the PMM is shown in [Figure 2-2](#).

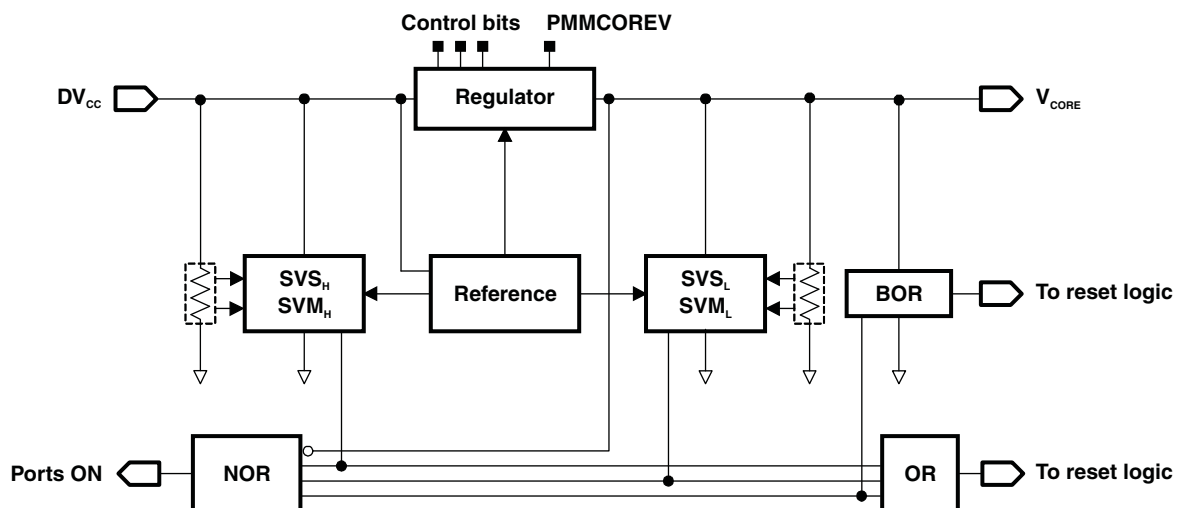


Figure 2-2. PMM Block Diagram

## 2.2 PMM Operation

### 2.2.1 $V_{\text{CORE}}$ and the Regulator

DV<sub>CC</sub> can be powered from a wide input voltage range, but the core logic of the device must be kept at a voltage lower than what this range allows. For this reason, a regulator has been integrated into the PMM. The regulator derives the necessary core voltage ( $V_{\text{CORE}}$ ) from DV<sub>CC</sub>.

Higher MCLK speeds require higher levels of  $V_{\text{CORE}}$ . Higher levels of  $V_{\text{CORE}}$  consume more power, and so the core voltage has been made programmable in up to four steps to allow it to provide only as much power as is required for a given MCLK setting. The level is controlled by the PMMCOREV bits. Note that the default setting, the lowest value of PMMCOREV, enables operation of MCLK over a very wide frequency range. As such, no PMM changes are required for many applications. See the device-specific data sheet for performance characteristics and core step levels supported.

Before increasing MCLK to a higher speed, it is necessary for software to ensure that the  $V_{\text{CORE}}$  level is sufficiently high for the chosen frequency. Failure to do so may force the CPU to attempt operation without sufficient power, which can cause unpredictable results. See [Section 2.2.4](#) for more information on the appropriate procedure to raise  $V_{\text{CORE}}$  for higher MCLK frequencies.

The regulator supports two different load settings to optimize power. The high-current mode is required when:

- The CPU is in active, LPM0, or LPM1 modes
- A clock source greater than 32 kHz is used to drive any module
- An interrupt is executed

Otherwise, the low-current mode is used. The hardware controls the load settings automatically, according to the criteria above.

### 2.2.2 Supply Voltage Supervisor and Monitor

The high-side supervisor and monitor (SVS<sub>H</sub> and SVM<sub>H</sub>) oversee DV<sub>CC</sub>, and the low-side supervisor and monitor (SVS<sub>L</sub> and SVM<sub>L</sub>) oversee  $V_{\text{CORE}}$ . By default, all of these modules are active, but each can be disabled using the corresponding enable bit (SVSHE, SVMHE, SVSLE, SVMLE), resulting in some power savings.

Typical application scenarios for supply voltage supervisors and monitors are:

- High-Side Supervisor, SVSH
  - Supervision of external power supply (DVCC)
  - Device reset because of low battery or supply voltage
- High-Side Monitor, SVMH
  - Monitoring of external power supply (DVCC)
  - Detection of low battery voltage (Pre-warning)
- Low-Side Supervisor, SVSL
  - Supervision of internal core voltage used to supply digital core
  - Device reset because of disruptive conditions at external V<sub>CORE</sub> pin (for example a short). The internal core voltage never drops below a critical level if parasitic events at the external V<sub>CORE</sub> pin are avoided.
- Low-Side Monitor, SVML
  - Monitoring of internal core voltage used to supply digital core
  - Detection of correct internal voltage levels when changing (especially increasing) the core voltage level before changing, for example, to higher system frequencies (also see [Section 2.2.4](#)).

#### 2.2.2.1 SVS and SVM Thresholds

The voltage thresholds enforced by the SVS and SVM modules are selectable. [Table 2-1](#) shows the SVS and SVM threshold registers, the voltage threshold they control, and the number of threshold options.

**Table 2-1. SVS and SVM Thresholds**

| Register | Description                                                     | Threshold                               | Available Steps  |
|----------|-----------------------------------------------------------------|-----------------------------------------|------------------|
| SVSHRVL  | SVS <sub>H</sub> reset voltage level                            | SVS <sub>H_IT-</sub>                    | 4                |
| SVSMHRRL | SVS <sub>H</sub> , SVM <sub>H</sub> reset release voltage level | SVS <sub>H_IT+</sub> , SVM <sub>H</sub> | 8                |
| SVSLRVL  | SVS <sub>L</sub> reset voltage level                            | SVS <sub>L_IT-</sub>                    | 4                |
| SVSMLRRL | SVS <sub>L</sub> , SVM <sub>L</sub> reset release voltage level | SVS <sub>L_IT+</sub> , SVM <sub>L</sub> | 4 <sup>(1)</sup> |

<sup>(1)</sup> The register settings support up to eight levels (0 through 7); however, levels 3 through 7 are identical.

### 2.2.2.1.1 Recommended SVS<sub>L</sub> Settings

For each of the core voltages, there are two supply voltage supervisor levels available. The SVSLRVL bits define the voltage level of VCORE below which the reset is activated. The SVSMLRRL bits define the voltage level of VCORE at which the reset is released. Although various settings can be chosen, there is one set of SVSLRVL and SVSMLRRL settings that is well suited for each core voltage selected by PMMCOREV. By default, an SVS<sub>L</sub> event always generates a POR (SVSLPE = 1), and it is recommended to always configure SVSLPE = 1 for reliable device startup. The most commonly used and recommended settings are shown in [Table 2-2](#).

**Table 2-2. Recommended SVS<sub>L</sub> Settings**

| PMMCOREV[1:0] | DVCC (V) | SVSLRVL[1:0]<br>Sets SVS <sub>L_IT-</sub> Level | SVSMLRRL[2:0]<br>Sets SVS <sub>L_IT+</sub> and SVM <sub>L</sub><br>levels |
|---------------|----------|-------------------------------------------------|---------------------------------------------------------------------------|
| 00            | ≥ 1.8    | 00                                              | 000                                                                       |
| 01            | ≥ 2.0    | 01                                              | 001                                                                       |
| 10            | ≥ 2.2    | 10                                              | 010                                                                       |
| 11            | ≥ 2.4    | 11                                              | 011                                                                       |

### 2.2.2.1.1.1 Recommended SVS<sub>H</sub> Settings

For the high-side supply, there are two supply voltage supervisor levels available. The SVSMHRRL bits define the voltage level of DVCC at which the reset is released. The SVSHRVL register defines the voltage level of DVCC below which the reset is turned on. These settings should be selected according to the minimum voltages required for device operation in a given application, as well as system power supply characteristics. See the device-specific data sheet for threshold values corresponding to the settings shown here. Although various settings are available, the most common are based on the maximum frequency required which, in turn, determines the minimum DVCC level supervised. By default, an SVS<sub>H</sub> event always generates a POR (SVSHPE = 1), and it is recommended to always configure SVSHPE = 1 for reliable device startup. The most commonly used and recommended settings are shown in [Table 2-3](#).

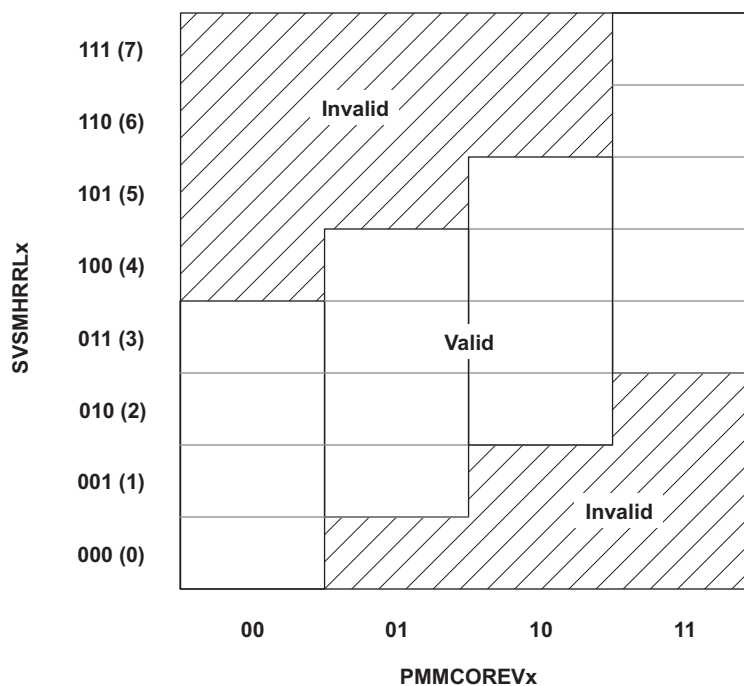
**Table 2-3. Recommended SVS<sub>H</sub> Settings**

| f <sub>SYS</sub> Max<br>(MHz) | DVCC<br>(V) | SVSHRVL[1:0]<br>Sets SVS <sub>H_IT-</sub> Level | SVSMHRRL[2:0]<br>Sets SVS <sub>H_IT+</sub> and<br>SVM <sub>H</sub> Levels | PMMCOREV[1:0] |
|-------------------------------|-------------|-------------------------------------------------|---------------------------------------------------------------------------|---------------|
| 8                             | >1.8        | 00                                              | 000                                                                       | 00            |
| 12                            | >2.0        | 01                                              | 001                                                                       | 01            |
| 20                            | >2.2        | 10                                              | 010                                                                       | 10            |
| 25                            | >2.4        | 11                                              | 011                                                                       | 11            |

The available voltage threshold settings of SVS<sub>H</sub> and SVM<sub>H</sub> are dependent on the voltage level setting of VCORE. [Table 2-4](#) summarizes all the possible settings available. All other settings not listed are invalid and should not be used. [Figure 2-3](#) shows the available settings for the SVM<sub>H</sub>.

**Table 2-4. Available SVS<sub>H</sub> and SVM<sub>H</sub> Settings Versus V<sub>CORE</sub> Settings**

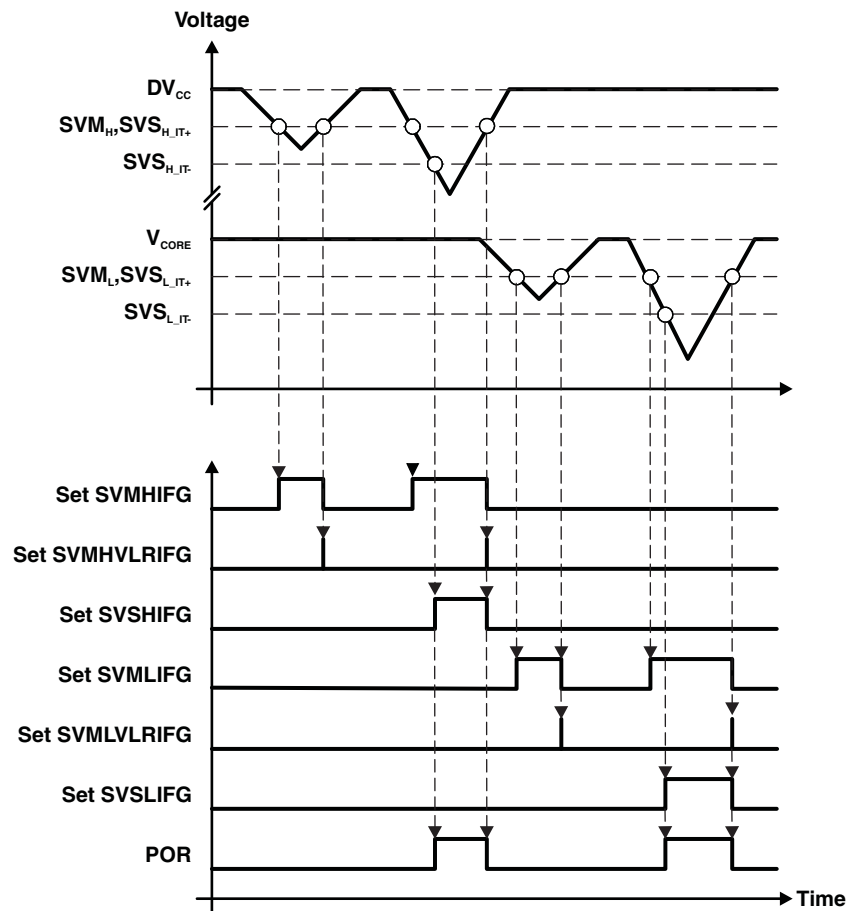
| PMMCOREV[1:0] | SVSHRVL[1:0]<br>Sets SVS <sub>H,IT</sub> Level | SVSMHRRL[2:0]<br>Sets SVS <sub>H,IT+</sub> and SVM <sub>H</sub> Levels |
|---------------|------------------------------------------------|------------------------------------------------------------------------|
| 00            | 00 through 11                                  | 000 through 011                                                        |
| 01            | 00 through 11                                  | 001 through 100                                                        |
| 10            | 00 through 11                                  | 010 through 101                                                        |
| 11            | 00 through 11                                  | 011 through 111                                                        |



**Figure 2-3. Available SVM<sub>H</sub> Settings Versus V<sub>CORE</sub> Settings**

The behavior of the SVS and SVM according to these thresholds is best portrayed graphically. [Figure 2-4](#) shows how the supervisors and monitors respond to various supply failure conditions.

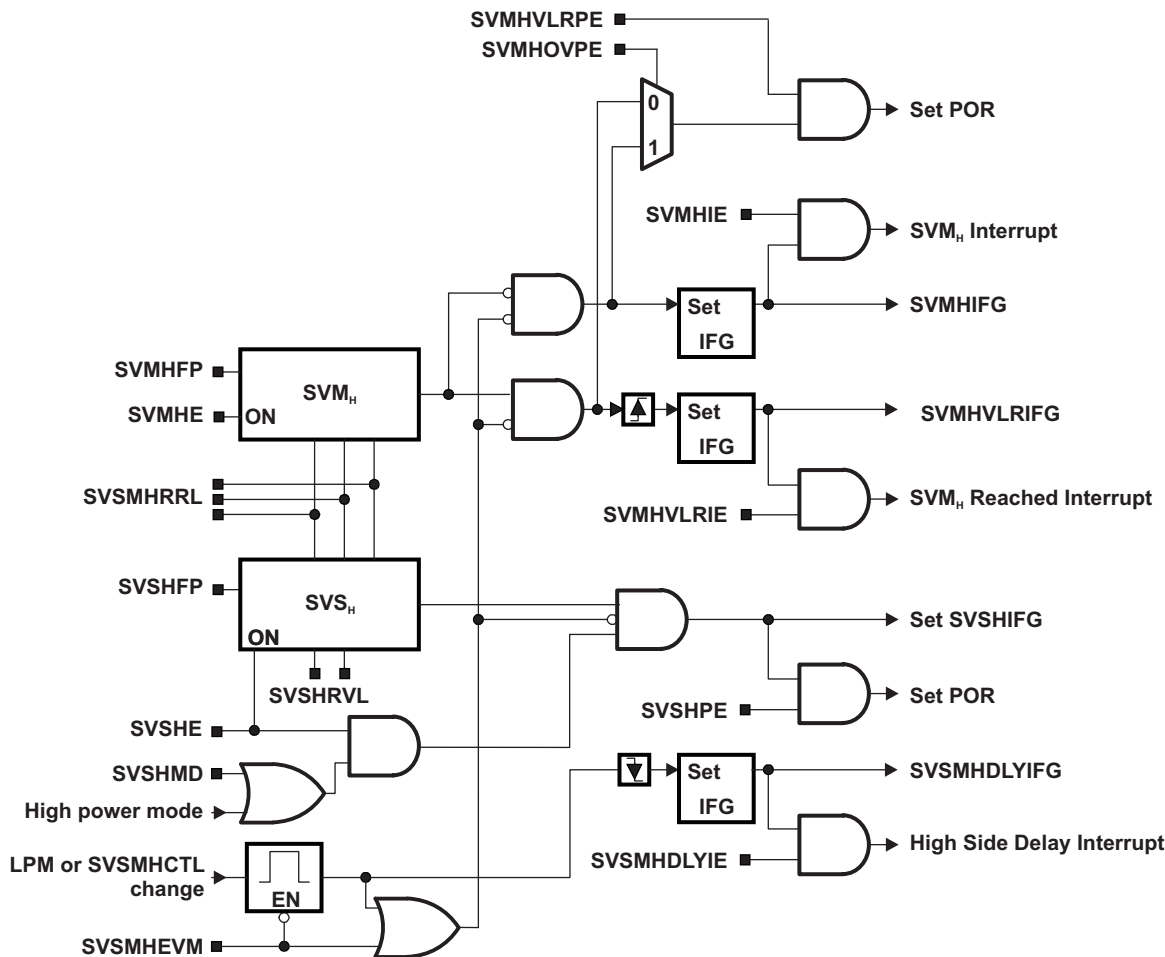
As [Figure 2-4](#) shows, there is hysteresis built into the supervision thresholds, such that the thresholds in force depend on whether the voltage rail is going up or down. There is no hysteresis in the monitoring thresholds.



**Figure 2-4. High-Side and Low-Side Voltage Failure and Resulting PMM Actions**

### 2.2.2.2 High-Side Supervisor (SVS<sub>H</sub>) and High-Side Monitor (SVM<sub>H</sub>)

The SVS<sub>H</sub> and SVM<sub>H</sub> modules are enabled by default. They can be disabled by clearing the SVSHE and SVMHE bits, respectively. Their block diagrams are shown in [Figure 2-5](#).



### Figure 2-5. High-Side SVS and SVM

If DV<sub>CC</sub> falls below the SVS<sub>H</sub> level, SVSHIFG (SVS<sub>H</sub> interrupt flag) is set. If DV<sub>CC</sub> remains below the SVS<sub>H</sub> level and software attempts to clear SVSHIFG, it is immediately set again by hardware. If the SVSHPE (SVS<sub>H</sub> POR enable) bit is set when SVSHIFG gets set, a POR is generated.

If DV<sub>CC</sub> falls below the SVM<sub>H</sub> level, SVMHIFG (SVM<sub>H</sub> interrupt flag) is set. If DV<sub>CC</sub> remains below the SVM<sub>H</sub> level and software attempts to clear SVMHIFG, it is immediately set again by hardware. If the SVMHIE (SVM<sub>H</sub> interrupt enable) bit is set when SVMHIFG gets set, an interrupt is generated. If a POR is desired when SVMHIFG is set, the SVM<sub>H</sub> can be configured to do so by setting the SVMHVLPE (SVM<sub>H</sub> voltage level reached POR enable) bit while SVMHOVPE bit is cleared.

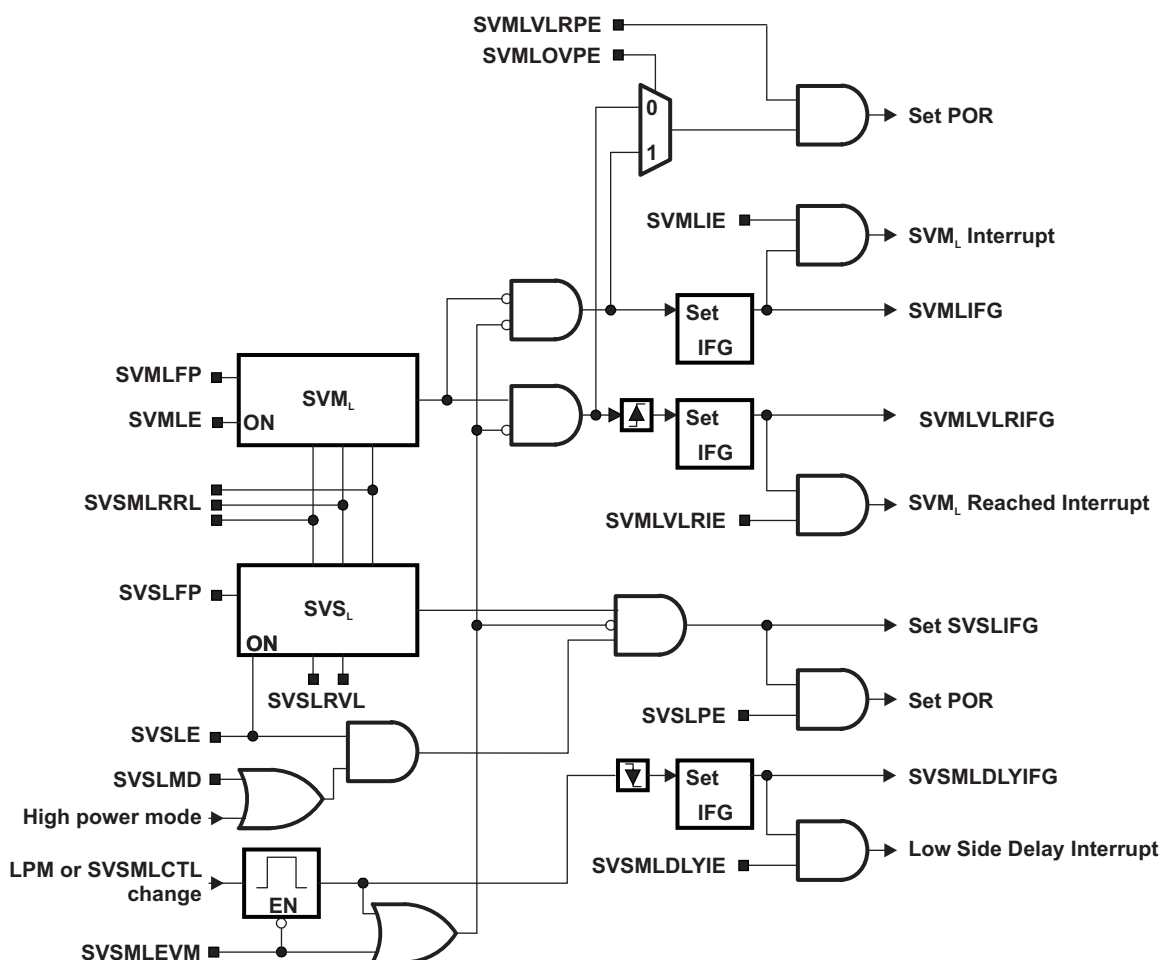
If DV<sub>CC</sub> rises above the SVM<sub>H</sub> level, the SVMHVLRIFG (SVM<sub>H</sub> voltage level reached) interrupt flag is set. If SVMHVLRIE (SVM<sub>H</sub> voltage level reached interrupt enable) is set when this occurs, an interrupt is also generated.

Alternatively the SVM<sub>H</sub> module can be used for overvoltage detection, but only with the highest core voltage setting (PMMCOREV = 11b), . This is accomplished by setting the SVMHOVPE (SVM<sub>H</sub> overvoltage POR enable) bit in addition to setting SVMHVLPE. Under these conditions, if a rising DVCC exceeds safe device operation, a POR is generated.

The SVS<sub>H</sub> and SVM<sub>H</sub> modules have configurable performance modes for power-saving operation. (See [Section 2.2.9](#) for more information.) If these SVS<sub>H</sub> and SVM<sub>H</sub> power modes are modified, or if a voltage level is modified, a delay element masks the interrupts and POR sources until the SVS<sub>H</sub> and SVM<sub>H</sub> circuits have settled. When SVSMHDLYST (delay status) reads zero, the delay has expired. In addition, the SVSMHDLYIFG (SVS<sub>H</sub> and SVM<sub>H</sub> delay expired) interrupt flag is set. If the SVSMHDLYIE (SVS<sub>H</sub> and SVM<sub>H</sub> delay expired interrupt enable) is set when this occurs, an interrupt is also generated.

All the interrupt flags of SVS<sub>H</sub> and SVM<sub>H</sub> remain set until cleared by a BOR or by software.

The SVS<sub>L</sub> and SVM<sub>L</sub> modules are enabled by default. They can be disabled by clearing SVSLE and SVMLE bits, respectively. Their block diagrams are shown in [Figure 2-6](#).



### Figure 2-6. Low-Side SVS and SVM

If  $V_{CORE}$  falls below the  $SVM_L$  level,  $SVMLIFG$  ( $SVM_L$  interrupt flag) is set. If  $V_{CORE}$  remains below the  $SVM_L$  level and software attempts to clear  $SVMLIFG$ , it is immediately set again by hardware. If the  $SVMLIE$  ( $SVM_L$  interrupt enable) bit is set when  $SVMLIFG$  gets set, an interrupt is generated. If a POR is desired when  $SVMLIFG$  is set, the  $SVM_L$  can be configured to do so by setting the  $SVMLVLRPE$  ( $SVM_L$  voltage level reached POR enable) bit while  $SVMLVPE$  bit is cleared.

If  $V_{CORE}$  rises above the  $SVM_L$  level, the  $SVMLVLRIFG$  ( $SVM_L$  voltage level reached) interrupt flag is set. If  $SVMLVLRIE$  ( $SVM_L$  voltage level reached interrupt enable) is set when this occurs, an interrupt is also generated.

The SVM<sub>L</sub> module can also be used for overvoltage detection. This is accomplished by setting the SVMLOVPE (SVM<sub>L</sub> overvoltage POR enable) bit, in addition to setting SVMLVLRPE. Under these conditions, if V<sub>CORE</sub> exceeds safe device operation, a POR is generated.

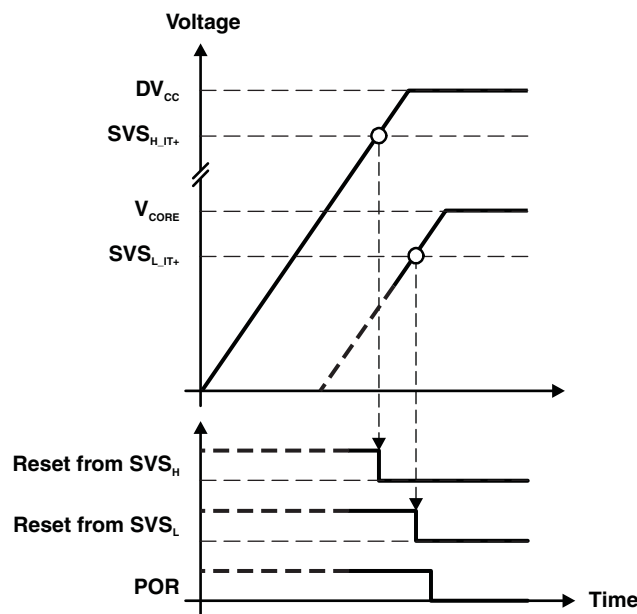
The SVS<sub>L</sub> and SVM<sub>L</sub> modules have configurable performance modes for power-saving operation. (See [Section 2.2.9](#) for more information.) If these SVS<sub>L</sub> and SVM<sub>L</sub> power modes are modified, or if a voltage level is modified, a delay element masks the interrupts and POR sources until the SVS<sub>L</sub> and SVM<sub>L</sub> circuits have settled. When SVSMLDLYST (delay status) reads zero, the delay has expired. In addition, the SVSMLDLYIFG (SVS<sub>L</sub>/SVM<sub>L</sub> delay expired) interrupt flag is set. If the SVSMLDLYIE (SVS<sub>L</sub>/SVM<sub>L</sub> delay expired interrupt enable) is set when this occurs, an interrupt is also generated.

In case of power-fail conditions, setting SVSLMD causes the SVS<sub>L</sub> interrupt flag to be set in LPM2, LPM3, and LPM4. If SVSLMD is not set, the SVS<sub>L</sub> interrupt flag is not set in LPM2, LPM3, and LPM4. In addition, all SVS<sub>L</sub> and SVM<sub>L</sub> events can be masked by setting SVSMLEVM. For most applications, SVSMLEVM should be cleared.

All the interrupt flags of SVS<sub>L</sub> and SVM<sub>L</sub> remain set until cleared by a BOR or by software.

### 2.2.3 Supply Voltage Supervisor and Monitor - Power-Up

When the device is powering up, the SVS<sub>H</sub> and SVS<sub>L</sub> functions are enabled by default. Initially, DV<sub>CC</sub> is low, and therefore the PMM holds the device in POR reset. When both the SVS<sub>H</sub> and SVS<sub>L</sub> levels are met, the reset is released. [Figure 2-7](#) shows this process.



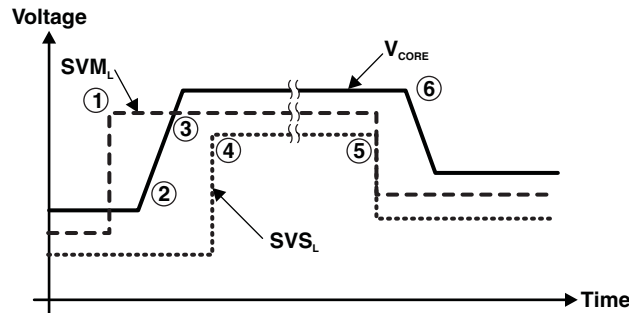
**Figure 2-7. PMM Action at Device Power-Up**

After this point, both voltage domains are supervised and monitored while the respective modules are enabled.

### 2.2.4 Increasing V<sub>CORE</sub> to Support Higher MCLK Frequencies

With a reset, V<sub>CORE</sub> and all the PMM thresholds, default to their lowest possible levels. These default settings allow a wide range of MCLK operation, and in many applications no change to these levels is required. However, if the application requires the performance provided by higher MCLK frequencies, software should ensure that V<sub>CORE</sub> has been raised to a sufficient voltage level before changing MCLK, since failing to supply sufficient voltage to the CPU could produce unpredictable results. For a given device, minimum V<sub>CORE</sub> levels required for maximum MCLK frequencies have been established (See the device data sheet for specific values).

After setting PMMCOREV to increase  $V_{\text{CORE}}$ , there is a time delay until the new voltage has been established. Software must not raise MCLK until the necessary core voltage has settled.  $\text{SVM}_L$  can be used to verify that  $V_{\text{CORE}}$  has met the required minimum value, prior to increasing MCLK. Figure 2-8 shows this procedure.



**Figure 2-8. Changing  $V_{\text{CORE}}$  and  $\text{SVM}_L$  and  $\text{SVS}_L$  Levels**

It is critical that the  $V_{\text{CORE}}$  level be increased by only one level at a time. The following steps 1 through 4 show the procedure to increase  $V_{\text{CORE}}$  by one level. This sequence is repeated to change the  $V_{\text{CORE}}$  level until the targeted level is obtained:

- Step 1: Program the  $\text{SVM}_H$  and  $\text{SVS}_H$  to the next level to ensure  $\text{DV}_{\text{CC}}$  is high enough for the next  $V_{\text{CORE}}$  level. Program the  $\text{SVM}_L$  to the next level and wait for ( $\text{SVSM LDLYIFG}$ ) to be set.
- Step 2: Program PMMCOREV to the next  $V_{\text{CORE}}$  level.
- Step 3: Wait for the voltage level reached ( $\text{SVMLVLRIFG}$ ) flag.
- Step 4: Program the  $\text{SVS}_L$  to the next level.

As a reference, the following is a C code example for increasing  $V_{\text{CORE}}$ . The sample libraries provide routines for increasing and decreasing the  $V_{\text{CORE}}$  and should be used whenever possible.

; C Code example for increasing core voltage.  
; Note: Change core voltage one level at a time.

```
void SetVCoreUp (unsigned int level)
{
    // Open PMM registers for write access
    PMMCTL0_H = 0xA5;
    // Make sure no flags are set for iterative sequences
    while ((PMMIFG & SVSMHDLYIFG) == 0);
    while ((PMMIFG & SVSMLDLYIFG) == 0);
    // Set SVS/SVM high side new level
    SVSMHCTL = SVSHE + SVSHRVL0 * level + SVMHE + SVSMHRRLO * level;
    // Set SVM low side to new level
    SVSMLCTL = SVSLE + SVMLE + SVSMLRRLO * level;
    // Wait till SVM is settled
    while ((PMMIFG & SVSMLDLYIFG) == 0);
    // Clear already set flags
    PMMIFG &= ~(SVMLVLRIFG + SVMLIFG);
    // Set VCore to new level
    PMMCTL0_L = PMMCOREV0 * level;
    // Wait till new level reached
    if ((PMMIFG & SVMLIFG))
        while ((PMMIFG & SVMLVLRIFG) == 0);
    // Set SVS/SVM low side to new level
    SVSMLCTL = SVSLE + SVSLRVL0 * level + SVMLE + SVSMLRRLO * level;
    // Lock PMM registers for write access
    PMMCTL0_H = 0x00;
}
```

---

**NOTE:** See the *MSP430x5xx and MSP430x6xx Core Libraries* ([SLAA448](#)). These libraries contain useful and ready-to-use functions for easily configuring and using the PMM module.

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### 2.2.5 Decreasing $V_{CORE}$ for Power Optimization

The risk posed by increasing MCLK frequency does not exist when decreasing MCLK from the current  $V_{CORE}$  or higher settings, because higher  $V_{CORE}$  levels can still support MCLK frequencies below the ones for which they were intended. However, significant power efficiency gains can be made by operating  $V_{CORE}$  at the lowest value required for a given MCLK frequency. It is critical that the  $V_{CORE}$  level be decreased by only one level at a time. The following steps show the procedure to decrease  $V_{CORE}$  by one level. This sequence is repeated to change the  $V_{CORE}$  level until the targeted level is obtained:

Steps 5 through 6 show the procedure to decrease  $V_{CORE}$ :

- Step 5: Program the  $SVM_L$  and  $SVS_L$  to the new level and wait for (SVSMLDLYIFG) to be set.
- Step 6: Program PMMCOREV to the new  $V_{CORE}$  level.

It is critical when lowering the  $V_{CORE}$  setting that the maximum MCLK frequency for the new  $V_{CORE}$  setting is not violated (see the device-specific data sheet).

### 2.2.6 Transition From LPM3 and LPM4 Modes to AM

The LDO requires time to settle when the application transitions from low-power modes to active modes. If a transition from LPM3 or LPM4 occurs and the device does not stay in active mode long enough, the LDO does not have time to settle sufficiently. Circuitry inside the LDO ensures that the LDO has its minimum required time to settle to its proper operating voltage. The circuitry ensures that every eighth transition from LPM3 or LPM4 causes the LDO to remain on long enough to properly settle. This is handled automatically and requires no setting by the application.

### 2.2.7 LPM3.5 and LPM4.5

LPM3.5 and LPM4.5 are additional low-power modes in which the regulator of the PMM is completely disabled, providing additional power savings. Not all devices support all LPMx.5 modes, so see the device-specific data sheet. Because there is no power supplied to  $V_{CORE}$  during LPMx.5, the CPU and all digital modules including RAM are unpowered. This disables the entire device and, as a result, the contents of the registers and RAM are lost. Any essential values should be stored to flash prior to entering LPMx.5. PMMREGOFF bit is used to disable the regulator. See the SYS module for complete descriptions and proper uses of LPMx.5.

Because the regulator of the PMM is disabled upon entering LPMx.5, all I/O register configurations are lost. Therefore, the configuration of I/O pins must be handled differently to ensure that all pins in the application behave in a controlled manner upon entering and exiting LPMx.5. Properly setting the I/O pins is critical to achieving the lowest possible power consumption in LPMx.5, as well as preventing any possible uncontrolled input or output I/O state in the application. The application has complete control of the I/O pin conditions preventing the possibility of unwanted spurious activity upon entry and exit from LPMx.5. The I/O pin state is held and locked based on the settings prior to LPMx.5 entry. Upon entry into LPMx.5, the LOCKLPM5 bit in PM5CTL0 of the PMM module is set automatically. Note that only the pin condition is retained. All other port configuration register settings are lost. See the Digital I/O chapter for further details.

### 2.2.8 Brownout Reset (BOR), Software BOR, Software POR

The primary function of the brownout reset (BOR) circuit occurs when the device is powering up. It is functional very early in the power-up ramp, generating a POR that initializes the system. It also functions when no SVS is enabled and a brownout condition occurs. It sustains this reset until the input power is sufficient for the logic, for proper reset of the system.

In an application, it may be desired to cause a BOR via software. Setting PMMSWBOR causes a software-driven BOR. PMMBORIFG is set accordingly. Note that a BOR also initiates a POR and PUC. PMMBORIFG can be cleared by software or by reading SYSRSTIV. Similarly, it is possible to cause a POR via software by setting PMMSWPOR. PMMPORIFG is set accordingly. A POR also initiates a PUC. PMMPORIFG can be cleared by software or by reading SYSRSTIV. Both PMMSWBOR and PMMSWPOR are self clearing. See the SYS module for complete descriptions of BOR, POR, and PUC resets.

### 2.2.9 SVS and SVM Performance Modes and Wakeup Times

The supervisors/monitors can function in one of two modes: normal and full performance. The difference is a tradeoff in response time versus the power consumed; full-performance mode has a faster response time but consumes considerably more power than normal mode. Full-performance mode might be considered in applications in which the decoupling of the external power supply cannot adequately prevent fast spikes on DV<sub>CC</sub> from occurring, or when the application has a particular intolerance to failure. In such cases, full-performance mode provides an additional layer of protection.

There are two ways to control the performance mode: manual and automatic. In manual mode, the normal/full-performance selection is the same for every operational mode except LPMx.5 (the SVS and SVM are always disabled in LPMx.5). In this case, the normal or full-performance selection is made with the SVSHFP, SVMHFP, SVSLFP, or SVMLFP bit, for their respective modules.

In automatic mode, hardware changes the normal or full-performance selection depending on the operational mode in effect.

The wakeup time of the device from low-power modes is affected by the settings of the SVS<sub>L</sub> and SVM<sub>L</sub> performance modes as listed in [Table 2-6](#), [Table 2-7](#), [Table 2-8](#), and [Table 2-9](#). The wakeup time from low-power modes is not affected by the settings of the SVS<sub>H</sub> and SVM<sub>H</sub>. All wake-ups from LPMx.5 (LPM3.5 or LPM4.5), are defined by the data sheet parametric,  $t_{\text{WAKE-UP-LPM5}}$ , regardless of the performance modes for SVS<sub>L</sub> or SVM<sub>L</sub>, because these are disabled in LPMx.5.

The tables in [Section 2.2.9.1](#) and [Section 2.2.9.2](#) show the required settings to select the control and performance modes for SVS<sub>L</sub>, SVM<sub>L</sub>, SVS<sub>H</sub>, and SVM<sub>H</sub>.

---

#### NOTE: Low-Power Modes

Even if the CPU requests a specific low-power mode, the device might not go into that state because of modules requesting clocks that should be switched off or have higher frequencies or because of modules requesting a higher drive capability of the LDO. The low-power modes mentioned in the tables assume that the device is actually in the requested state; that is, no module is requesting a deviating clock setting or drive capability.

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## 2.2.9.1 Low-Side SVS and SVM Control and Performance Mode Selection

**Table 2-5. SVS<sub>L</sub> and SVM<sub>L</sub> Control Mode Selection**

| SVSMLACE | SVSLMD | SVS <sub>L</sub> Control Mode | SVM <sub>L</sub> Control Mode |
|----------|--------|-------------------------------|-------------------------------|
| 0        | 0      | Automatic (see Table 2-6)     | Manual (see Table 2-8)        |
| 0        | 1      | Manual (see Table 2-7)        | Manual (see Table 2-8)        |
| 1        | 0      | Automatic (see Table 2-6)     | Automatic (see Table 2-9)     |
| 1        | 1      | Automatic (see Table 2-6)     | Automatic (see Table 2-9)     |

**Table 2-6. SVS<sub>L</sub> Automatic Performance Control**

| SVSLE | SVSLMD | SVSLFP | AM, LPM0, LPM1<br>SVS <sub>L</sub> State | LPM2, LPM3, LPM4<br>SVS <sub>L</sub> State | Wakeup Time<br>LPM2, LPM3, LPM4 |
|-------|--------|--------|------------------------------------------|--------------------------------------------|---------------------------------|
| 0     | x      | x      | Off                                      | Off                                        | t <sub>WAKE-UP-FAST</sub>       |
| 1     | 0      | 0      | Normal                                   | Off                                        | t <sub>WAKE-UP-SLOW</sub>       |
| 1     | 0      | 1      | Full performance                         | Off                                        | t <sub>WAKE-UP-FAST</sub>       |
| 1     | 1      | 0      | Normal                                   | Off                                        | t <sub>WAKE-UP-SLOW</sub>       |
| 1     | 1      | 1      | Full performance                         | Normal                                     | t <sub>WAKE-UP-FAST</sub>       |

**Table 2-7. SVS<sub>L</sub> Manual Performance Modes**

| SVSLE |  | SVSLFP | AM, LPM0, LPM1<br>SVS <sub>L</sub> State | LPM2, LPM3, LPM4<br>SVS <sub>L</sub> State | Wakeup Time<br>LPM2, LPM3, LPM4 |
|-------|--|--------|------------------------------------------|--------------------------------------------|---------------------------------|
| 0     |  | x      | Off                                      | Off                                        | t <sub>WAKE-UP-FAST</sub>       |
| 1     |  | 0      | Normal                                   | Normal                                     | t <sub>WAKE-UP-SLOW</sub>       |
| 1     |  | 1      | Full performance                         | Full performance                           | t <sub>WAKE-UP-FAST</sub>       |

**Table 2-8. SVM<sub>L</sub> Automatic Performance Control**

| SVMLE |  | SVMLFP | AM, LPM0, LPM1<br>SVM <sub>L</sub> State | LPM2, LPM3, LPM4<br>SVM <sub>L</sub> State | Wakeup Time<br>LPM2, LPM3, LPM4 |
|-------|--|--------|------------------------------------------|--------------------------------------------|---------------------------------|
| 0     |  | x      | Off                                      | Off                                        | t <sub>WAKE-UP-FAST</sub>       |
| 1     |  | 0      | Normal                                   | Off                                        | t <sub>WAKE-UP-SLOW</sub>       |
| 1     |  | 1      | Full performance                         | Normal                                     | t <sub>WAKE-UP-FAST</sub>       |

**Table 2-9. SVM<sub>L</sub> Manual Performance Modes**

| SVMLE |  | SVMLFP | AM, LPM0, LPM1<br>SVM <sub>L</sub> State | LPM2, LPM3, LPM4<br>SVM <sub>L</sub> State | Wakeup Time<br>LPM2, LPM3, LPM4 |
|-------|--|--------|------------------------------------------|--------------------------------------------|---------------------------------|
| 0     |  | x      | Off                                      | Off                                        | t <sub>WAKE-UP-FAST</sub>       |
| 1     |  | 0      | Normal                                   | Normal                                     | t <sub>WAKE-UP-SLOW</sub>       |
| 1     |  | 1      | Full performance                         | Full performance                           | t <sub>WAKE-UP-FAST</sub>       |

### 2.2.9.2 High-Side SVS and SVM Control and Performance Mode Selection

**Table 2-10. SVS<sub>H</sub> and SVM<sub>H</sub> Control Mode Selection**

| SVSMHACE | SVSHMD | SVS <sub>H</sub> Control Mode               | SVM <sub>H</sub> Control Mode               |
|----------|--------|---------------------------------------------|---------------------------------------------|
| 0        | 0      | Automatic (see <a href="#">Table 2-11</a> ) | Manual (see <a href="#">Table 2-13</a> )    |
| 0        | 1      | Manual (see <a href="#">Table 2-12</a> )    | Manual (see <a href="#">Table 2-13</a> )    |
| 1        | 0      | Automatic (see <a href="#">Table 2-11</a> ) | Automatic (see <a href="#">Table 2-14</a> ) |
| 1        | 1      | Automatic (see <a href="#">Table 2-11</a> ) | Automatic (see <a href="#">Table 2-14</a> ) |

**Table 2-11. SVS<sub>H</sub> Automatic Performance Control**

| SVSHE | SVSHMD | SVSHFP | AM, LPM0, LPM1<br>SVS <sub>H</sub> State | LPM2, LPM3, LPM4<br>SVS <sub>H</sub> State |
|-------|--------|--------|------------------------------------------|--------------------------------------------|
| 0     | x      | x      | Off                                      | Off                                        |
| 1     | 0      | 0      | Normal                                   | Off                                        |
| 1     | 0      | 1      | Full performance                         | Off                                        |
| 1     | 1      | 0      | Normal                                   | Off                                        |
| 1     | 1      | 1      | Full performance                         | Normal                                     |

**Table 2-12. SVS<sub>H</sub> Manual Performance Modes**

| SVSHE |  | SVSHFP | AM, LPM0, LPM1<br>SVS <sub>H</sub> State | LPM2, LPM3, LPM4<br>SVS <sub>H</sub> State |
|-------|--|--------|------------------------------------------|--------------------------------------------|
| 0     |  | x      | Off                                      | Off                                        |
| 1     |  | 0      | Normal                                   | Normal                                     |
| 1     |  | 1      | Full performance                         | Full performance                           |

**Table 2-13. SVM<sub>H</sub> Automatic Performance Control**

| SVMHE |  | SVMHFP | AM, LPM0, LPM1<br>SVM <sub>H</sub> State | LPM2, LPM3, LPM4<br>SVM <sub>H</sub> State |
|-------|--|--------|------------------------------------------|--------------------------------------------|
| 0     |  | x      | Off                                      | Off                                        |
| 1     |  | 0      | Normal                                   | Off                                        |
| 1     |  | 1      | Full performance                         | Normal                                     |

**Table 2-14. SVM<sub>H</sub> Manual Performance Modes**

| SVMHE |  | SVMHFP | AM, LPM0, LPM1<br>SVM <sub>H</sub> State | LPM2, LPM3, LPM4<br>SVM <sub>H</sub> State |
|-------|--|--------|------------------------------------------|--------------------------------------------|
| 0     |  | x      | Off                                      | Off                                        |
| 1     |  | 0      | Normal                                   | Normal                                     |
| 1     |  | 1      | Full performance                         | Full performance                           |

### 2.2.9.3 Wakeup Times in Debug Mode

The TEST/SBWTCK pin is used for interfacing to the development tools via Spy-Bi-Wire and JTAG. When the TEST/SBWTCK pin is high, wakeup times from LPM2, LPM3, and LPM4 may be different compared to when TEST/SBWTCK is low. When the TEST/SBWTCK pin is high, all delays associated with the SVS<sub>L</sub> and SVM<sub>L</sub> settings have no effect and the device wakes within  $t_{\text{WAKE-UP-FAST}}$ . Pay careful attention to the real-time behavior when exiting from LPM2, LPM3, and LPM4 with the device connected to a development tool (for example, MSP-FET430UIF).

### **2.2.10 PMM Interrupts**

Interrupt flags generated by the PMM are routed to the system NMI interrupt vector generator register, SYSSNIV. When the PMM causes a reset, a value is generated in the system reset interrupt vector generator register, SYSRSTIV, corresponding to the source of the reset. These registers are defined within the SYS module. More information on the relationship between the PMM and SYS modules is available in the SYS chapter.

### **2.2.11 Port I/O Control**

The PMM provides a means of ensuring that I/O pins cannot behave in uncontrolled fashion during an undervoltage event. During these times, outputs are disabled, both normal drive and the weak pullup/pulldown function. If the CPU is functioning normally, and then an undervoltage event occurs, any pin configured as an input has its PxIN register value locked in at the point the event occurs, until voltage is restored. During the undervoltage event, external voltage changes on the pin are not registered internally. This helps prevent erratic behavior from occurring.

### **2.2.12 Supply Voltage Monitor Output (SVMOUT, Optional)**

The state of SVMLIFG, SVMLVLRIFG, SVMHIFG, and SVMLVLRIFG can be monitored on the external SVMOUT pin. Each of these interrupt flags can be enabled (SVMLOE, SVMLVLROE, SVMHOE, SVMLVLROE) to generate an output signal. The polarity of the output is selected by the SVMOUTPOL bit. If SVMOUTPOL is set, the output is set to 1 if an enabled interrupt flag is set.

## 2.3 PMM Registers

The PMM registers are listed in [Table 2-15](#). The base address of the PMM module can be found in the device-specific data sheet. The address offset of each PMM register is given in [Table 2-15](#). The password, PMMPW, defined in the PMMCTL0 register controls access to all PMM, SVS, and SVM registers. Once the correct password is written, the write access is enabled. The write access is disabled by writing a wrong password in byte mode to the PMMCTL0 upper byte. Word accesses to PMMCTL0 with a wrong password triggers a PUC. A write access to a register other than PMMCTL0 while write access is not enabled causes a PUC.

**NOTE:** All registers have word or byte register access. For a generic register *ANYREG*, the suffix "\_L" (*ANYREG\_L*) refers to the lower byte of the register (bits 0 through 7). The suffix "\_H" (*ANYREG\_H*) refers to the upper byte of the register (bits 8 through 15).

**Table 2-15. PMM Registers**

| Offset | Acronym    | Register Name                                | Type       | Access | Reset | Section                       |
|--------|------------|----------------------------------------------|------------|--------|-------|-------------------------------|
| 00h    | PMMCTL0    | PMM control register 0                       | Read/write | Word   | 9600h | <a href="#">Section 2.3.1</a> |
| 00h    | PMMCTL0_L  |                                              | Read/write | Byte   | 00h   |                               |
| 01h    | PMMCTL0_H  |                                              | Read/write | Byte   | 96h   |                               |
| 02h    | PMMCTL1    | PMM control register 1                       | Read/write | Word   | 0000h | <a href="#">Section 2.3.2</a> |
| 02h    | PMMCTL1_L  |                                              | Read/write | Byte   | 00h   |                               |
| 03h    | PMMCTL1_H  |                                              | Read/write | Byte   | 00h   |                               |
| 04h    | SVSMHCTL   | SVS and SVM high side control register       | Read/write | Word   | 4400h | <a href="#">Section 2.3.3</a> |
| 04h    | SVSMHCTL_L |                                              | Read/write | Byte   | 00h   |                               |
| 05h    | SVSMHCTL_H |                                              | Read/write | Byte   | 44h   |                               |
| 06h    | SVSMLCTL   | SVS and SVM low side control register        | Read/write | Word   | 4400h | <a href="#">Section 2.3.4</a> |
| 06h    | SVSMLCTL_L |                                              | Read/write | Byte   | 00h   |                               |
| 07h    | SVSMLCTL_H |                                              | Read/write | Byte   | 44h   |                               |
| 08h    | SVSMIO     | SVSIN and SVMOUT control register (optional) | Read/write | Word   | 0020h | <a href="#">Section 2.3.5</a> |
| 08h    | SVSMIO_L   |                                              | Read/write | Byte   | 20h   |                               |
| 09h    | SVSMIO_H   |                                              | Read/write | Byte   | 00h   |                               |
| 0Ch    | PMMIFG     | PMM interrupt flag register                  | Read/write | Word   | 0000h | <a href="#">Section 2.3.6</a> |
| 0Ch    | PMMIFG_L   |                                              | Read/write | Byte   | 00h   |                               |
| 0Dh    | PMMIFG_H   |                                              | Read/write | Byte   | 00h   |                               |
| 0Eh    | PMMRIE     | PMM interrupt enable register                | Read/write | Word   | 1100h | <a href="#">Section 2.3.7</a> |
| 0Eh    | PMMRIE_L   |                                              | Read/write | Byte   | 00h   |                               |
| 0Fh    | PMMRIE_H   |                                              | Read/write | Byte   | 11h   |                               |
| 10h    | PM5CTL0    | Power mode 5 control register 0              | Read/write | Word   | 0000h | <a href="#">Section 2.3.8</a> |
| 10h    | PM5CTL0_L  |                                              | Read/write | Byte   | 00h   |                               |
| 11h    | PM5CTL0_H  |                                              | Read/write | Byte   | 00h   |                               |

### 2.3.1 PMMCTL0 Register

Power Management Module Control Register 0

**Figure 2-9. PMMCTL0 Register**

|          |          |      |           |          |          |          |        |
|----------|----------|------|-----------|----------|----------|----------|--------|
| 15       | 14       | 13   | 12        | 11       | 10       | 9        | 8      |
| PMPW     |          |      |           |          |          |          |        |
| rw-1     | rw-0     | rw-0 | rw-1      | rw-0     | rw-1     | rw-1     | rw-0   |
| 7        | 6        | 5    | 4         | 3        | 2        | 1        | 0      |
| PMMHPMRE | Reserved |      | PMMREGOFF | PMMSWPOR | PMMSWBOR | PMMCOREV |        |
| rw-0     | r-0      | r-0  | rw-0      | rw-0     | rw-0     | rw-[0]   | rw-[0] |

**Table 2-16. PMMCTL0 Register Description**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                 |
|------|-----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15-8 | PMPW      | RW   | 96h   | PMM password. Always read as 096h. When using word operations, must be written with 0A5h or a PUC is generated. When using byte operation, writing 0A5h unlocks all PMM registers. When using byte operation, writing anything different than 0A5h locks all PMM registers. |
| 7    | PMMHPMRE  | RW   | 0h    | Global high power module request enable. If the PMMHPMRE bit is set, any module is able to request the PMM high-power mode.                                                                                                                                                 |
| 6-5  | Reserved  | R    | 0h    | Reserved. Always reads as 0.                                                                                                                                                                                                                                                |
| 4    | PMMREGOFF | RW   | 0h    | Regulator off (see the SYS chapter for details)                                                                                                                                                                                                                             |
| 3    | PMMSWPOR  | RW   | 0h    | Software power-on reset. Setting this bit to 1 triggers a POR. This bit is self clearing.                                                                                                                                                                                   |
| 2    | PMMSWBOR  | RW   | 0h    | Software brownout reset. Setting this bit to 1 triggers a BOR. This bit is self clearing.                                                                                                                                                                                   |
| 1-0  | PMMCOREV  | RW   | 0h    | Core voltage (see the device-specific data sheet for supported levels and corresponding voltages)<br>00b = V(CORE) level 0<br>01b = V(CORE) level 1<br>10b = V(CORE) level 2<br>11b = V(CORE) level 3                                                                       |

### 2.3.2 PMMCTL1 Register

Power Management Module Control Register 1

**Figure 2-10. PMMCTL1 Register**

|          |     |          |        |          |     |          |      |
|----------|-----|----------|--------|----------|-----|----------|------|
| 15       | 14  | 13       | 12     | 11       | 10  | 9        | 8    |
| Reserved |     |          |        |          |     |          |      |
| r-0      | r-0 | r-0      | r-0    | r-0      | r-0 | r-0      | r-0  |
| 7        | 6   | 5        | 4      | 3        | 2   | 1        | 0    |
| Reserved |     | Reserved |        | Reserved |     | Reserved |      |
| r-0      | r-0 | rw-[0]   | rw-[0] | r-0      | r-0 | rw-0     | rw-0 |

**Table 2-17. PMMCTL1 Register Description**

| Bit  | Field    | Type | Reset | Description                              |
|------|----------|------|-------|------------------------------------------|
| 15-6 | Reserved | R    | 0h    | Reserved. Always reads as 0.             |
| 5-4  | Reserved | RW   | 0h    | Reserved. Must always be written with 0. |
| 3-2  | Reserved | R    | 0h    | Reserved. Always reads as 0.             |
| 1-0  | Reserved | RW   | 0h    | Reserved. Must always be written with 0. |

### 2.3.3 SVSMHCTL Register

Supply Voltage Supervisor and Monitor High-Side Control Register

**Figure 2-11. SVSMHCTL Register**

|          |          |          |          |            |          |         |        |
|----------|----------|----------|----------|------------|----------|---------|--------|
| 15       | 14       | 13       | 12       | 11         | 10       | 9       | 8      |
| SVMHFP   | SVMHE    | Reserved | SVMHOVPE | SVSHFP     | SVSHE    | SVSHRVL |        |
| rw-[0]   | rw-1     | r-0      | rw-[0]   | rw-[0]     | rw-1     | rw-[0]  | rw-[0] |
| 7        | 6        | 5        | 4        | 3          | 2        | 1       | 0      |
| SVSMHACE | SVSMHEVM | Reserved | SVSHMD   | SVSMHDLYST | SVSMHRRL |         |        |
| rw-[0]   | rw-0     | r-0      | rw-0     | r-0        | rw-[0]   | rw-[0]  | rw-[0] |

**Table 2-18. SVSMHCTL Register Description**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                   |
|-----|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | SVMHFP     | RW   | 0h    | SVM high-side full-performance mode. If this bit is set, the SVMH operates in full-performance mode.<br>0b = Normal mode. See the device-specific data sheet for response times.<br>1b = Full-performance mode. See the device-specific data sheet for response times.                                                                                                        |
| 14  | SVMHE      | RW   | 1h    | SVM high-side enable. If this bit is set, the SVMH is enabled.                                                                                                                                                                                                                                                                                                                |
| 13  | Reserved   | R    | 0h    | Reserved. Always reads as 0.                                                                                                                                                                                                                                                                                                                                                  |
| 12  | SVMHOVPE   | RW   | 0h    | SVM high-side overvoltage enable. If this bit is set, the SVMH overvoltage detection is enabled. If SVMHVLPE is also set, a POR occurs on an overvoltage condition.                                                                                                                                                                                                           |
| 11  | SVSHFP     | RW   | 0h    | SVS high-side full-performance mode. If this bit is set, the SVSH operates in full-performance mode.<br>0b = Normal mode. See the device-specific data sheet for response times.<br>1b = Full-performance mode. See the device-specific data sheet for response times.                                                                                                        |
| 10  | SVSHE      | RW   | 1h    | SVS high-side enable. If this bit is set, the SVSH is enabled.                                                                                                                                                                                                                                                                                                                |
| 9-8 | SVSHRVL    | RW   | 0h    | SVS high-side reset voltage level. If DVCC falls short of the SVSH voltage level selected by SVSHRVL, a reset is triggered (if SVSHPE = 1). The voltage levels are defined in the device-specific data sheet.                                                                                                                                                                 |
| 7   | SVSMHACE   | RW   | 0h    | SVS and SVM high-side automatic control enable. If this bit is set, the low-power mode of the SVSH and SVMH circuits is under hardware control.                                                                                                                                                                                                                               |
| 6   | SVSMHEVM   | RW   | 0h    | SVS and SVM high-side event mask. If this bit is set, the SVSH and SVMH events are masked.<br>0b = No events are masked.<br>1b = All events are masked.                                                                                                                                                                                                                       |
| 5   | Reserved   | R    | 0h    | Reserved. Always reads as 0.                                                                                                                                                                                                                                                                                                                                                  |
| 4   | SVSHMD     | RW   | 0h    | SVS high-side mode. If this bit is set, the SVSH interrupt flag is set in LPM2, LPM3, and LPM4 in case of power-fail conditions. If this bit is not set, the SVSH interrupt is not set in LPM2, LPM3, and LPM4.                                                                                                                                                               |
| 3   | SVSMHDLYST | RW   | 0h    | SVS and SVM high-side delay status. If this bit is set, the SVSH and SVMH events are masked for some delay time. The delay time depends on the power mode of the SVSH and SVMH. If SVMHFP = 1 and SVSHFP = 1 (that is, full-performance mode), the delay is shorter. See the device-specific data sheet for details. The bit is cleared by hardware if the delay has expired. |
| 2-0 | SVSMHRRL   | RW   | 0h    | SVS and SVM high-side reset release voltage level. These bits define the reset release voltage level of the SVSH. It is also used for the SVMH to define the voltage reached level. The voltage levels are defined in the device-specific data sheet.                                                                                                                         |

### 2.3.4 SVSMLCTL Register

Supply Voltage Supervisor and Monitor Low-Side Control Register

**Figure 2-12. SVSMLCTL Register**

|          |          |          |          |            |          |         |        |
|----------|----------|----------|----------|------------|----------|---------|--------|
| 15       | 14       | 13       | 12       | 11         | 10       | 9       | 8      |
| SVMLFP   | SVMLE    | Reserved | SVMLOVPE | SVSLFP     | SVSLE    | SVSLRVL |        |
| rw-[0]   | rw-1     | r-0      | rw-[0]   | rw-[0]     | rw-1     | rw-[0]  | rw-[0] |
| 7        | 6        | 5        | 4        | 3          | 2        | 1       | 0      |
| SVSMLACE | SVSMLEVM | Reserved | SVSLMD   | SVSMLDLYST | SVSMLRRL |         |        |
| rw-[0]   | rw-0     | r-0      | rw-0     | r-0        | rw-[0]   | rw-[0]  | rw-[0] |

**Table 2-19. SVSMLCTL Register Description**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                 |
|-----|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | SVMLFP     | RW   | 0h    | SVML low-side full-performance mode. If this bit is set, the SVML operates in full-performance mode.<br>0b = Normal mode. See the device-specific data sheet for response times.<br>1b = Full-performance mode. See the device-specific data sheet for response times.                                                      |
| 14  | SVMLE      | RW   | 1h    | SVML low-side enable. If this bit is set, the SVML is enabled.                                                                                                                                                                                                                                                              |
| 13  | Reserved   | R    | 0h    | Reserved. Always reads as 0.                                                                                                                                                                                                                                                                                                |
| 12  | SVMLOVPE   | RW   | 0h    | SVML low-side overvoltage enable. If this bit is set, the SVML overvoltage detection is enabled.                                                                                                                                                                                                                            |
| 11  | SVSLFP     | RW   | 0h    | SVSL low-side full-performance mode. If this bit is set, the SVSL operates in full-performance mode.<br>0b = Normal mode. See the device-specific data sheet for response times.<br>1b = Full-performance mode. See the device-specific data sheet for response times.                                                      |
| 10  | SVSLE      | RW   | 1h    | SVSL low-side enable. If this bit is set, the SVSL is enabled.                                                                                                                                                                                                                                                              |
| 9-8 | SVSLRVL    | RW   | 0h    | SVSL low-side reset voltage level. If V(CORE) falls short of the SVSL voltage level selected by SVSLRVL, a reset is triggered (if SVSLPE = 1).                                                                                                                                                                              |
| 7   | SVSMLACE   | RW   | 0h    | SVSL and SVML low-side automatic control enable. If this bit is set, the low-power mode of the SVSL and SVML circuits is under hardware control.                                                                                                                                                                            |
| 6   | SVSMLEVM   | RW   | 0h    | SVSL and SVML low-side event mask. If this bit is set, the SVSL and SVML events are masked.<br>0b = No events are masked.<br>1b = All events are masked.                                                                                                                                                                    |
| 5   | Reserved   | R    | 0h    | Reserved. Always reads as 0.                                                                                                                                                                                                                                                                                                |
| 4   | SVSLMD     | RW   | 0h    | SVSL low-side mode. If this bit is set, the SVSL interrupt flag is set in LPM2, LPM3 and LPM4 in case of power-fail conditions. If this bit is not set, the SVSL interrupt is not set in LPM2, LPM3, and LPM4.                                                                                                              |
| 3   | SVSMLDLYST | RW   | 0h    | SVSL and SVML low-side delay status. If this bit is set, the SVSL and SVML events are masked for a delay time. The delay time depends on the power mode of the SVSL and SVML. If SVMLFP = 1 and SVSLFP = 1 (that is, full-performance mode), the delay is shorter. The bit is cleared by hardware if the delay has expired. |
| 2-0 | SVSMLRRL   | RW   | 0h    | SVSL and SVML low-side reset release voltage level. These bits define the reset release voltage level of the SVSL. It is also used for the SVML to define the voltage reached level.                                                                                                                                        |

### 2.3.5 SVSMIO Register

SVSIN and SVMOUT Control Register

**Figure 2-13. SVSMIO Register**

|          |     |           |           |        |          |     |     |
|----------|-----|-----------|-----------|--------|----------|-----|-----|
| 15       | 14  | 13        | 12        | 11     | 10       | 9   | 8   |
| Reserved |     |           | SVMHVLROE | SVMHOE | Reserved |     |     |
| r-0      | r-0 | r-0       | rw-[0]    | rw-[0] | r-0      | r-0 | r-0 |
| 7        | 6   | 5         | 4         | 3      | 2        | 1   | 0   |
| Reserved |     | SVMOUTPOL | SVMLVLROE | SVMLOE | Reserved |     |     |
| r-0      | r-0 | rw-[1]    | rw-[0]    | rw-[0] | r-0      | r-0 | r-0 |

**Table 2-20. SVSMIO Register Description**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                         |
|-------|-----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15-13 | Reserved  | R    | 0h    | Reserved. Always reads as 0.                                                                                                                                                                        |
| 12    | SVMHVLROE | RW   | 0h    | SVM high-side voltage level reached output enable. If this bit is set, the SVMHVLRIFG bit is output to the device SVMOUT pin. The device-specific port logic has to be configured accordingly.      |
| 11    | SVMHOE    | RW   | 0h    | SVM high-side output enable. If this bit is set, the SVMHIFG bit is output to the device SVMOUT pin. The device-specific port logic has to be configured accordingly.                               |
| 10-6  | Reserved  | R    | 0h    | Reserved. Always reads as 0.                                                                                                                                                                        |
| 5     | SVMOUTPOL | RW   | 1h    | SVMOUT pin polarity. If this bit is set, SVMOUT is active high. An error condition is signaled by a 1 at SVMOUT. If SVMOUTPOL is cleared, the error condition is signaled by a 0 at the SVMOUT pin. |
| 4     | SVMLVLROE | RW   | 0h    | SVM low-side voltage level reached output enable. If this bit is set, the SVMLVLRIFG bit is output to the device SVMOUT pin. The device-specific port logic has to be configured accordingly.       |
| 3     | SVMLOE    | RW   | 0h    | SVM low-side output enable. If this bit is set, the SVMLIFG bit is output to the device SVMOUT pin. The device-specific port logic has to be configured accordingly.                                |
| 2-0   | Reserved  | R    | 0h    | Reserved. Always reads as 0.                                                                                                                                                                        |

### 2.3.6 PMMIFG Register

Power Management Module Interrupt Flag Register

**Figure 2-14. PMMIFG Register**

| 15         | 14                        | 13                     | 12                     | 11       | 10                        | 9         | 8           |
|------------|---------------------------|------------------------|------------------------|----------|---------------------------|-----------|-------------|
| PMMLPM5IFG | Reserved                  | SVSLIFG <sup>(1)</sup> | SVSHIFG <sup>(1)</sup> | Reserved | PMMPORIFG                 | PMMRSTIFG | PMMBORIFG   |
| rw-[0]     | r-0                       | rw-[0]                 | rw-[0]                 | r-0      | rw-[0]                    | rw-[0]    | rw-[0]      |
| 7          | 6                         | 5                      | 4                      | 3        | 2                         | 1         | 0           |
| Reserved   | SVMHVLRIFG <sup>(1)</sup> | SVMHIFG                | SVSMHDLYIFG            | Reserved | SVMLVLRIFG <sup>(1)</sup> | SVMLIFG   | SVSMLDLYIFG |
| r-0        | rw-[0]                    | rw-[0]                 | rw-0                   | r-0      | rw-[0]                    | rw-[0]    | rw-0        |

<sup>(1)</sup> After power up, the reset value depends on the power sequence.

<sup>(1)</sup> After power up, the reset value depends on the power sequence.

**Table 2-21. PMMIFG Register Description**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | PMMLPM5IFG | RW   | 0h    | LPMx.5 flag. This bit is set if the system was in LPMx.5 before. The bit is cleared by software or by reading the reset vector word. A power failure on the DVCC domain clears the bit.<br>0b = No interrupt pending<br>1b = Interrupt pending         |
| 14  | Reserved   | R    | 0h    | Reserved. Always reads as 0.                                                                                                                                                                                                                           |
| 13  | SVSLIFG    | RW   | 0h    | SVS low-side interrupt flag. The bit is cleared by software or by reading the reset vector word.<br>0b = No interrupt pending<br>1b = Interrupt pending                                                                                                |
| 12  | SVSHIFG    | RW   | 0h    | SVS high-side interrupt flag. The bit is cleared by software or by reading the reset vector word.<br>0b = No interrupt pending<br>1b = Interrupt pending                                                                                               |
| 11  | Reserved   | R    | 0h    | Reserved. Always reads as 0.                                                                                                                                                                                                                           |
| 10  | PMMPORIFG  | RW   | 0h    | PMM software power-on reset interrupt flag. This interrupt flag is set if a software POR is triggered. The bit is cleared by software or by reading the reset vector word, SYSRSTIV.<br>0b = No interrupt pending<br>1b = Interrupt pending            |
| 9   | PMMRSTIFG  | RW   | 0h    | PMM reset pin interrupt flag. This interrupt flag is set if the RST/NMI pin is the reset source. The bit is cleared by software or by reading the reset vector word.<br>0b = No interrupt pending<br>1b = Interrupt pending                            |
| 8   | PMMBORIFG  | RW   | 0h    | PMM software brownout reset interrupt flag. This interrupt flag is set if a software BOR (PMMSWBOR) is triggered. The bit is cleared by software or by reading the reset vector word, SYSRSTIV.<br>0b = No interrupt pending<br>1b = Interrupt pending |
| 7   | Reserved   | R    | 0h    | Reserved. Always reads as 0.                                                                                                                                                                                                                           |
| 6   | SVMHVLRIFG | RW   | 0h    | SVM high-side voltage level reached interrupt flag. The bit is cleared by software or by reading the reset vector (SVSHPE = 1) word or by reading the interrupt vector (SVSHPE = 0) word.<br>0b = No interrupt pending<br>1b = Interrupt pending       |
| 5   | SVMHIFG    | RW   | 0h    | SVM high-side interrupt flag. The bit is cleared by software.<br>0b = No interrupt pending<br>1b = Interrupt pending                                                                                                                                   |

**Table 2-21. PMMIFG Register Description (continued)**

| Bit | Field       | Type | Reset | Description                                                                                                                                                                                                                                     |
|-----|-------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | SVSMHDLYIFG | RW   | 0h    | SVS and SVM high-side delay expired interrupt flag. This interrupt flag is set if the delay element expired. The bit is cleared by software or by reading the interrupt vector word.<br>0b = No interrupt pending<br>1b = Interrupt pending     |
| 3   | Reserved    | R    | 0h    | Reserved. Always reads as 0.                                                                                                                                                                                                                    |
| 2   | SVMLVLRIFG  | RW   | 0h    | SVM low-side voltage level reached interrupt flag. The bit is cleared by software or by reading the reset vector (SVSLPE = 1) word or by reading the interrupt vector (SVSLPE = 0) word.<br>0b = No interrupt pending<br>1b = Interrupt pending |
| 1   | SVMLIFG     | RW   | 0h    | SVM low-side interrupt flag. The bit is cleared by software.<br>0b = No interrupt pending<br>1b = Interrupt pending                                                                                                                             |
| 0   | SVSMLDLYIFG | RW   | 0h    | SVS and SVM low-side delay expired interrupt flag. This interrupt flag is set if the delay element expired. The bit is cleared by software or by reading the interrupt vector word.<br>0b = No interrupt pending<br>1b = Interrupt pending      |

### 2.3.7 PMMRIE Register

Power Management Module Reset and Interrupt Enable Register

**Figure 2-15. PMMRIE Register**

|          |            |            |            |          |            |            |            |
|----------|------------|------------|------------|----------|------------|------------|------------|
| 15       | 14         | 13         | 12         | 11       | 10         | 9          | 8          |
| Reserved |            | SVMHVL RPE | SVSHPE     | Reserved |            | SVMLVL RPE | SVSLPE     |
| r-0      | r-0        | rw-[0]     | rw-[1]     | r-0      | r-0        | rw-[0]     | rw-[1]     |
| 7        | 6          | 5          | 4          | 3        | 2          | 1          | 0          |
| Reserved | SVMHVL RIE | SVMHIE     | SVSMHDLYIE | Reserved | SVMLVL RIE | SVMLIE     | SVSMLDLYIE |
| r-0      | rw-0       | rw-0       | rw-0       | r-0      | rw-0       | rw-0       | rw-0       |

**Table 2-22. PMMRIE Register Description**

| Bit   | Field      | Type | Reset | Description                                                                                                                     |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 15-14 | Reserved   | R    | 0h    | Reserved. Always reads as 0.                                                                                                    |
| 13    | SVMHVL RPE | RW   | 0h    | SVM high-side voltage level reached power-on reset enable. If this bit is set, exceeding the SVMH voltage level triggers a POR. |
| 12    | SVSHPE     | RW   | 1h    | SVS high-side power-on reset enable. If this bit is set, falling below the SVSH voltage level triggers a POR.                   |
| 11-10 | Reserved   | R    | 0h    | Reserved. Always reads as 0.                                                                                                    |
| 9     | SVMLVL RPE | RW   | 0h    | SVM low-side voltage level reached power-on reset enable. If this bit is set, exceeding the SVML voltage level triggers a POR.  |
| 8     | SVSLPE     | RW   | 1h    | SVS low-side power-on reset enable. If this bit is set, falling below the SVSL voltage level triggers a POR.                    |
| 7     | Reserved   | R    | 0h    | Reserved. Always reads as 0.                                                                                                    |
| 6     | SVMHVL RIE | RW   | 0h    | SVM high-side reset voltage level interrupt enable                                                                              |
| 5     | SVMHIE     | RW   | 0h    | SVM high-side interrupt enable. This bit is cleared by software or if the interrupt vector word is read.                        |
| 4     | SVSMHDLYIE | RW   | 0h    | SVS and SVM high-side delay expired interrupt enable                                                                            |
| 3     | Reserved   | R    | 0h    | Reserved. Always reads as 0.                                                                                                    |
| 2     | SVMLVL RIE | RW   | 0h    | SVM low-side reset voltage level interrupt enable                                                                               |
| 1     | SVMLIE     | RW   | 0h    | SVM low-side interrupt enable. This bit is cleared by software or if the interrupt vector word is read.                         |
| 0     | SVSMLDLYIE | RW   | 0h    | SVS and SVM low-side delay expired interrupt enable                                                                             |

### 2.3.8 PM5CTL0 Register

Power Mode 5 Control Register 0

**Figure 2-16. PM5CTL0 Register**

|          |    |    |    |    |    |    |          |
|----------|----|----|----|----|----|----|----------|
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8        |
| Reserved |    |    |    |    |    |    |          |
| r0       | r0 | r0 | r0 | r0 | r0 | r0 | r0       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0        |
| Reserved |    |    |    |    |    |    | LOCKLPM5 |
| r0       | r0 | r0 | r0 | r0 | r0 | r0 | rw-[0]   |

**Table 2-23. PM5CTL0 Register Description**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15-1 | Reserved | R    | 0h    | Reserved. Always reads as 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 0    | LOCKLPM5 | RW   | 0h    | <p>Lock I/O pin configuration upon entry to or exit from LPMx.5. When power is applied to the device, this bit, once set, can only be cleared by the user or via another power cycle.</p> <p>Note: This bit was formerly named LOCKIO, and some application reports and code examples may continue to use this terminology.</p> <p>0b = I/O pin configuration is not locked and defaults to its reset condition.</p> <p>1b = I/O pin configuration remains locked. Pin state is held during LPMx.5 entry and exit.</p> |