Power Management Module (PMM) and Supply Voltage Supervisor (SVS)

This chapter describes the operation of the Power Management Module (PMM) and Supply Voltage Supervisor (SVS).

Topic **Page**

2.1 Power Management Module (PMM) Introduction

PMM features include:

- Wide supply voltage (DV_{CC}) range: 1.8 V to 3.6 V
- Generation of voltage for the device core (V_{CORE})
- Supply voltage supervisor (SVS) for DV_{CC}
- Brownout reset (BOR)
- Software accessible power-fail indicators
- I/O protection during power-fail condition
- Reference voltage output on external pin
- Shared reference systems (device specific)
  - Basic shared reference systems: 1.5-V on-chip reference
  - Enhanced shared reference systems: 1.5-V, 2.0-V, or 2.5-V on-chip reference

The PMM manages all functions related to the power supply and its supervision for the device. Its primary functions are, first, to generate a supply voltage for the core logic and, second, to provide several mechanisms for the supervision of the voltage applied to the device (DV_{CC}).

The PMM uses an integrated low-dropout voltage regulator (LDO) to produce a secondary core voltage (V_{CORE}) from the primary one applied to the device (DV_{CC}). In general, V_{CORE} supplies the CPU, memories, and the digital modules, while DV_{CC} supplies the I/Os and analog modules. The V_{CORE} output is maintained using a dedicated voltage reference. The input or primary side of the regulator is referred to in this chapter as its high side. The output or secondary side is referred to in this chapter as its low side.

The block diagram of the PMM is shown in Figure 2-1.

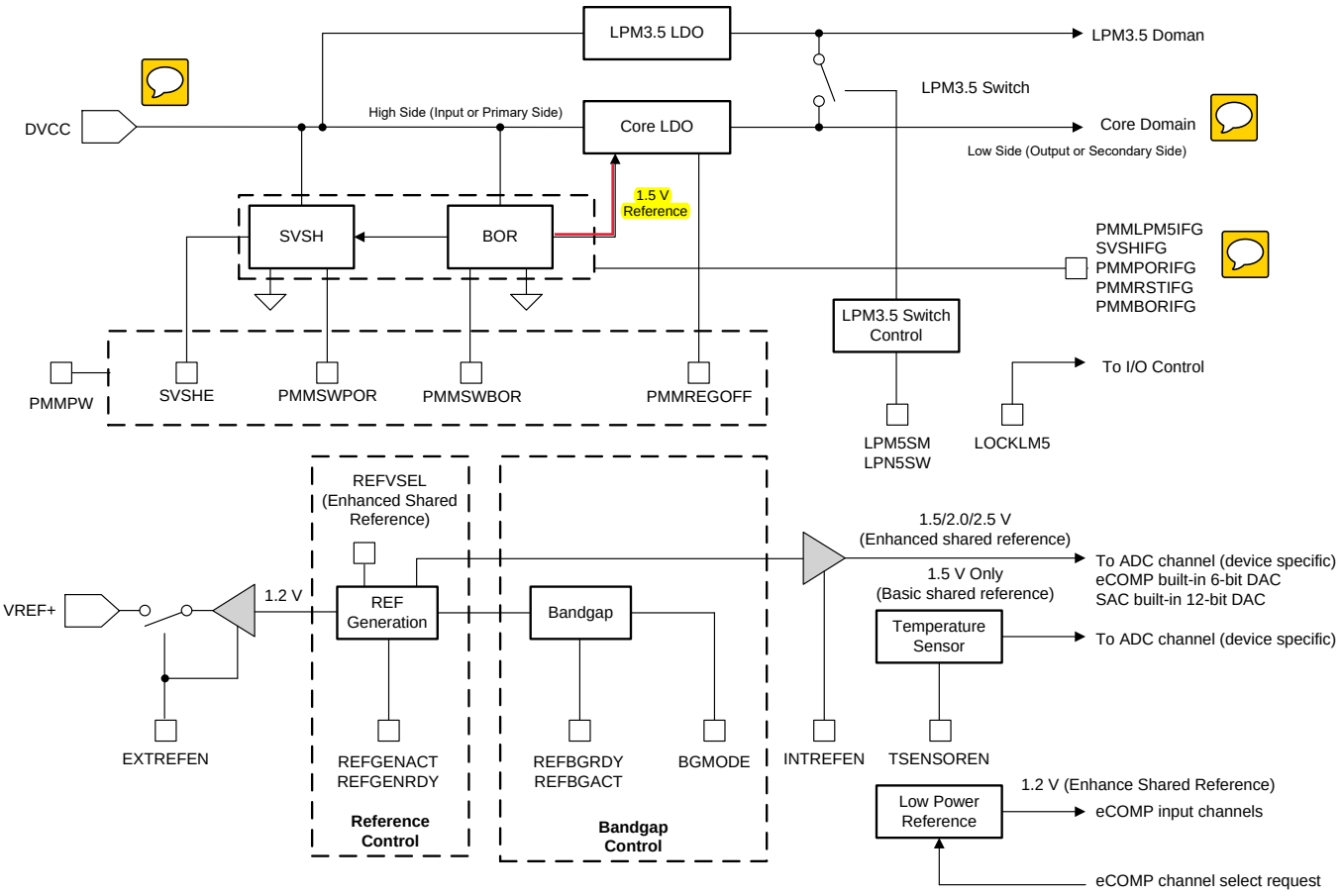

Figure 2-1. PMM Block Diagram

2.2 PMM Operation

2.2.1 V_{CORE} and the Regulator

DV_{CC} can be powered from a wide input voltage range, but the core logic of the device must be kept at a voltage lower than what this range allows. For this reason, a regulator (LDO) has been integrated into the PMM. The regulator derives the necessary core voltage (V_{CORE}) from DV_{CC}.

The regulator supports different load settings to optimize power. The hardware controls the load settings automatically, according to the following criteria:

- Selected and active power modes
- Selected and active clocks
- Clock frequencies according to Clock System (CS) settings
- JTAG or SBW is active

In addition to the main LDO, an ultra-low-power regulator (RTC LDO) provides a regulated voltage to the real-time clock module (including the 32-kHz crystal oscillator) and other ultra-low-power modules that remain active during LPM3.5 when the main LDO is switched off.

2.2.2 Supply Voltage Supervisor

The high-side supervisor (SVSH) oversees DV_{CC}. It is active in all power modes by default. In LPM3, LPM4, LPM3.5, and LPM4.5, it can be disabled by setting SVSHE = 0.

2.2.2.1 SVS Thresholds

As Figure 2-2 shows, there is hysteresis built into the supervision thresholds, so that which threshold is in force depends on whether the voltage rail is rising or falling.

The behavior of the SVS according to these thresholds is best portrayed graphically. Figure 2-2 shows how the supervisors respond to various supply failure conditions.

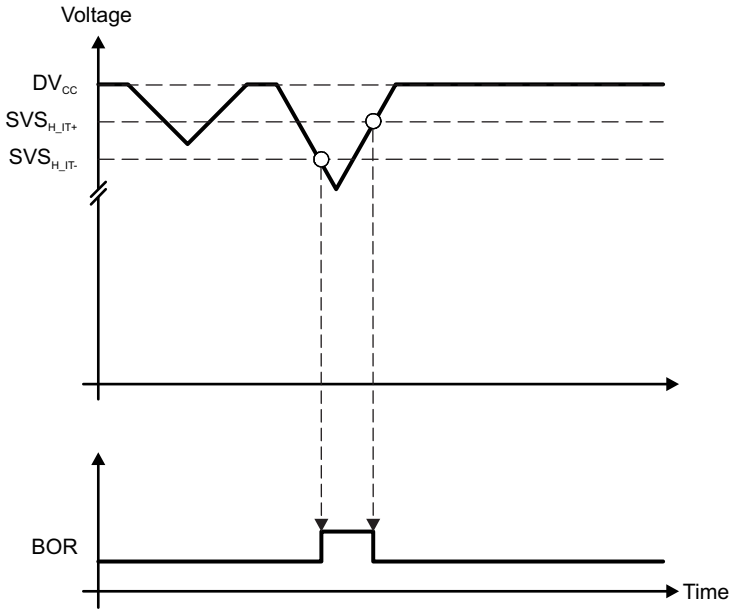

Figure 2-2. Voltage Failure and Resulting PMM Actions

2.2.3 Supply Voltage Supervisor During Power-Up

When the device is powering up, the SVSH function is enabled by default. Initially, DV_{CC} is low, and therefore the PMM holds the device in BOR reset. When the SVSH level is met, the reset is released. Figure 2-3 shows this process.

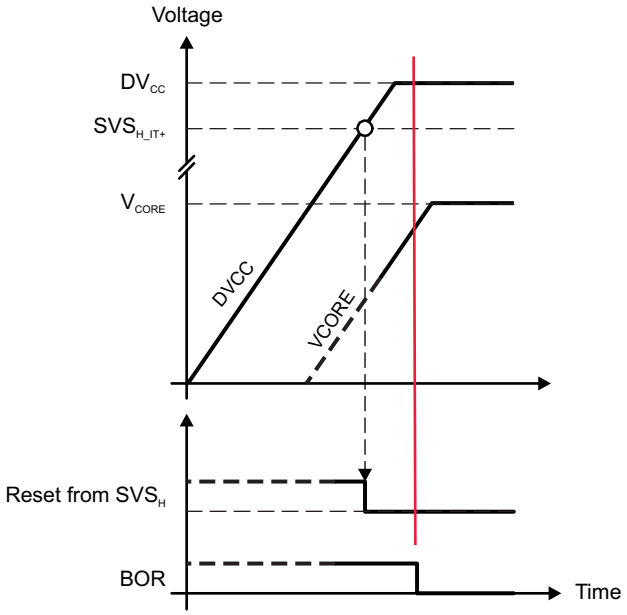

Figure 2-3. PMM Action at Device Power-Up

2.2.4 LPM3.5 and LPM4.5 (LPMx.5)

LPM3.5 and LPM4.5 are low-power modes in which the core voltage regulator of the PMM is completely disabled to provide additional power savings. Because there is no power supplied to V_{CORE} during LPMx.5, the CPU and all digital modules including RAM are unpowered. This essentially disables the entire device and, as a result, the contents of the registers and RAM are lost. Any essential values should be stored to FRAM prior to entering LPMx.5. See the SYS module for complete description and uses of LPMx.5.

LPM3.5 and LPM4.5 can be configured with SVS enabled (SVSHE = 1) or with SVS disabled (SVSHE = 0). Disabling the SVS results in lower power consumption, whereas enabling it provides the ability to detect supply drops and getting a "wake-up" due to the supply drop below the SVS threshold. Note, the "wake-up" due to a supply failure would not be flagged as a LPMx.5 wake-up but as a SVS reset event. In LPM4.5, enabling the SVS also results in approximately 10 times faster start-up time than with disabled SVS.

2.2.5 Low-Power Reset

In battery-operated applications, it might be desirable to limit the current drawn by the device to a minimum after the supply drops below the SVS power-down level. By default, as soon as the supply voltage drops below the SVS power-down level, the complete device is reset and prepared to return into active mode quickly when the supply voltage becomes available again. This state results in a current consumption of approximately 50 µA to 100 µA (typical).

Pulling the reset pin during the LPM4.5 low-power reset state causes the device to enter its default reset state (with higher current consumption), and the device starts up when the supply rises above the SVS power-up level.

If the device is already in LPMx.5 (with SVS enabled) before the supply voltage drops below the SVS threshold, then the device automatically enters the low-power reset state (that is, the device enters LPM4.5 state with SVS, RTC domain, and all wake-up events disabled). (In LPMx.5 the I/Os are already in a defined state. Therefore, no NMI handling is required to define the I/O states.)

2.2.6 Brownout Reset (BOR)

The primary function of the BOR circuit occurs when the device is powering up. It is functional very early in the power-up ramp, generating a BOR that initializes the system. It also functions when no SVS is enabled and a brownout condition occurs. It sustains this reset until the input power is sufficient for the logic and for proper reset of the system.

In an application, it may be desired to cause a BOR in software. Setting PMMSWBOR causes a software-driven BOR. PMMBORIFG is set accordingly. Note that a BOR also initiates a POR and PUC. PMMBORIFG can be cleared by software or by reading SYSRSTIV.

Similarly, it is possible to cause a POR in software by setting PMMSWPOR. PMMPORIFG is set accordingly. A POR also initiates a PUC. PMMPORIFG can be cleared by software or by reading SYSRSTIV. Both PMMSWBOR and PMMSWPOR are self clearing. See the SYS module for complete descriptions of BOR, POR, and PUC resets.

2.2.7 LPM3.5 Switch

The LPM3.5 switch supplies the LPM3.5 power domain with main LDO output, which allows the peripherals to consume more current and operate at high frequency. When the device enters LPM3.5, all peripherals in LPM3.5 domains are isolated from the core domain and fully supplied by the LPM3.5 LDO. The LPM3.5 switch can be either manually or automatically controlled. The LPM3.5 switch mode can be set by LPM5SM in the PM5CTL0 register.

In the automatic control mode (the LPM5SM bit is clear), all peripherals in LPM3.5 domains are automatically controlled by PMM depending on the dynamic loading. This is the recommended mode for general operation.

In the manual control mode (the LPM5SM bit is set), the LPM3.5 switch is specified by the LPM5SW bit in the PM5CTL0 register. When LPM5SW is set, the LPM3.5 switch is connected. When LPM5SW is clear, the LPM3.5 switch is disconnected. It is recommended to turn off the switch to avoid unnecessary leakage before the device enters LPM3.5. When the device recovers back from LPM3.5 mode, the switch should be turned on to offer sufficient current for high-frequency operation.

The LPM5SW defaults to logic 1, which means that the LPM3.5 switch is always connected after a BOR, POR, or PUC reset.

2.2.8 Shared Reference Generation and Distribution

The PMM module has a high-accuracy bandgap for various voltage references on the chip. The bandgap is automatically turned on and off depending on the operating mode. The REFBGRDY bit in the PMMCTL2 register reports the readiness of the bandgap. When REFBGRDY is set, the bandgap reference is ready for use.

In basic shared reference systems, two voltage references are generated for internal shared reference (1.5 V) and external reference (VREF+ pin, 1.2 V) use. The voltage generator is automatically controlled by the device in response to the voltage reference request (either internal or external). The REFGENACT and REFGENRDY bits represent the status of the generator status and report whether or not the output is at the specified voltage. The internal reference voltage (1.5 V) is internally connected to an ADC channel (see the data sheet for device-specific configuration). The INTREFEN bit in PMMCTL2 controls when the 1.5-V voltage is available on the specified ADC channel.

In enhanced shared reference systems, three voltage references are available for use: internal shared reference (1.5 V, 2.0 V, or 2.5 V), external reference (VREF+ pin, 1.2 V), and internal low-power reference (1.2 V). The voltage generator is automatically controlled by the device in response to the voltage reference request (either internal or external). The REFGENACT and REFGENRDY bits represent the status of the generator status and report whether or not the output is at the specified voltage. The internal shared reference (1.5 V, 2.0 V, or 2.5 V) is programmable by setting the REFVSEL bits in PMMCTL2. It is internally connected to an ADC channel (see the data sheet for device-specific configuration), the eCOMP built-in 6-bit DAC, and the SAC built-in 12-bit DAC. The INTREFEN bit in PMMCTL2 controls when the internal shared reference voltage is available to these modules.

The external reference voltage (1.2 V) is connected a given external ADC channel (refer to the data sheet for device-specific configuration). If this ADC channel is multiplexed with other functionality, the 1.2-V output function only works when the ADC is selected as the function on this pin. The EXTREFEN bit in PMMCTL2 controls if the 1.2-V voltage is available to the specified external ADC channel. The external reference voltage supports up to 1-mA drive capability.

In enhanced shared reference systems, an additional low-power 1.2-V reference is available for eCOMP operations. This reference can be activated by selecting eCOMP input channels.

2.2.9 Temperature Sensor

The PMM contains a built-in temperature sensor that software can use to monitor the die temperature for fault protection in high-temperature environments. The temperature sensor is internally connected to an ADC channel. The connection is device specific and can be found in the ADC section in the data sheet. The TSENSOREN bit in the PMMCTL2 register must be set to turn on the sensor before it is used. The temperature of 30°C is factory-trimmed. Therefore, any temperature to be measured can be calculated by Equation 11.

$$T = 0.00355 \times (V_T - V_{30ºC}) + 30ºC \quad (11)$$

2.2.10 $\overline{\text{RST}}$/NMI

The external $\overline{\text{RST}}$/NMI terminal is pulled low on a BOR reset condition. $\overline{\text{RST}}$/NMI can be used as reset source for the rest of the application.

2.2.11 PMM Interrupts

Interrupt flags generated by the PMM are routed to the system NMI interrupt vector generator register, SYSSNIV. When the PMM causes a reset, a value is generated in the system reset interrupt vector generator register, SYSRSTIV, corresponding to the source of the reset. These registers are defined within the SYS module. More information on the relationship between the PMM and SYS modules is available in the SYS chapter.

2.2.12 Port I/O Control

The PMM ensures that I/O pins cannot behave in uncontrolled fashion during an undervoltage event. During these times, outputs are disabled, including both the normal drive and the weak pullup and pulldown functions. If the CPU is functioning normally before an undervoltage event occurs, any pin configured as an input has its PxIN register value latched when the event occurs, until voltage is restored. During the undervoltage event, external voltage changes on the pin are not registered internally. This helps prevent erratic behavior.

2.3 PMM Registers

Table 2-1 shows the PMM registers and their address offsets. The base address of the PMM module can be found in the device-specific data sheet.

The password defined in the PMMCTL0 register controls access to all PMM registers except PM5CTL0. PM5CTL0 can be accessed without the password. After the correct password is written, write access is enabled (this includes byte access to the PMMCTL0 lower byte). Write access is disabled by writing a wrong password in byte mode to the PMMCTL0 upper byte. Word access to PMMCTL0 with a wrong password causes a PUC. Write access to a register other than PMMCTL0 while write access is not enabled causes a PUC.

NOTE: All registers have word or byte register access. For a generic register *ANYREG*, the suffix "_L" (*ANYREG_L*) refers to the lower byte of the register (bits 0 through 7). The suffix "_H" (*ANYREG_H*) refers to the upper byte of the register (bits 8 through 15).

Table 2-1. PMM Registers

Offset	Acronym	Register Name	Type	Access	Reset	Section
00h	PMMCTL0	PMM control register 0	Read/write	Word	9640h	Section 2.3.1
00h	PMMCTL0_L		Read/write	Byte	40h	
01h	PMMCTL0_H		Read/write	Byte	96h	
02h	PMMCTL1	PMM control register 1	Read/write(1)	Word	9600h	Section 2.3.2
02h	PMMCTL1_L		Read(1)	Byte	00h	
03h	PMMCTL1_H		Read(1)	Byte	96h	
04h	PMMCTL2	PMM control register 2	Read/write	Word	0000h	Section 2.3.3
04h	PMMCTL2_L		Read/write	Byte	00h	
05h	PMMCTL2_H		Read/write	Byte	00h	
0Ah	PMMIFG	PMM interrupt flag register	Read/write	Word	0000h	Section 2.3.5
0Ah	PMMIFG_L		Read/write	Byte	00h	
0Bh	PMMIFG_H		Read/write	Byte	00h	
0Eh	PMMIE	PMM interrupt enable register	Read/write	Word	0000h	Section 2.3.4
0Eh	PMMIE_L		Read/write	Byte	00h	
0Fh	PMMIE_H		Read/write	Byte	00h	
10h	PM5CTL0	Power mode 5 control register 0	Read/write	Word	0011h	Section 2.3.6
10h	PM5CTL0_L		Read/write	Byte	11h	
11h	PM5CTL0_H		Read/write	Byte	00h	

(1) PMMCTL1 can be written as word only.

2.3.1 PMMCTL0 Register (offset = 00h) [reset = 9640h]

Power Management Module Control Register 0

Figure 2-4. PMMCTL0 Register

15	14	13	12	11	10	9	8
PMMPW							
rw-1	rw-0	rw-0	rw-1	rw-0	rw-1	rw-1	rw-0
7	6	5	4	3	2	1	0
Reserved	SVSHE	Reserved	PMMREGOFF	PMMSWPOR	PMMSWBOR	Reserved	
rw-[0]	rw-[1]	r0	rw-[0]	rw-(0)	rw-[0]	r0	r0

Table 2-2. PMMCTL0 Register Description

Bit	Field	Type	Reset	Description
15-8	PMMPW	RW	96h	PMM password. Always reads as 096h. Write with 0A5h to unlock the PMM registers.
7	Reserved	RW	0h	Reserved. Must be written with 0.
6	SVSHE	RW	1h	High-side SVS enable. 0b = High-side SVS (SVSH) is disabled in LPM2, LPM3, LPM4, LPM3.5, and LPM4.5. SVSH is enabled in active mode, LPM0, and LPM1. 1b = SVSH is always enabled.
5	Reserved	R	0h	Reserved. Always reads as 0
4	PMMREGOFF	RW	0h	Regulator off 0b = Regulator remains on when going into LPM3 or LPM4 1b = Regulator is turned off when going to LPM3 or LPM4. System enters LPM3.5 or LPM4.5, respectively.
3	PMMSWPOR	RW	0h	Software POR. Set this bit to 1 to trigger a POR. This bit is self clearing. 0b = Normal operation 1b = Set to 1 to trigger a POR
2	PMMSWBOR	RW	0h	Software brownout reset. Set this bit to 1 to trigger a BOR. This bit is self clearing. 0b = Normal operation 1b = Set to 1 to trigger a BOR
1-0	Reserved	R	0h	Reserved. Always reads as 0.

2.3.2 PMMCTL1 Register (offset = 02h) [reset = 0000h]

Power Management Module Control Register 1

Figure 2-5. PMMCTL1 Register

15	14	13	12	11	10	9	8
Reserved							
rw-1	rw-0	rw-0	rw-1	rw-0	rw-1	rw-1	rw-0
7	6	5	4	3	2	1	0
Reserved							
rw-[0]	rw-[0]	rw-[0]	rw-[0]	rw-[0]	rw-[0]	rw-[0]	r0

Table 2-3. PMMCTL1 Register Description

Bit	Field	Type	Reset	Description
15-0	Reserved	R	9600h	Reserved. Always reads as 9600h.

2.3.3 PMMCTL2 Register (offset = 04h) [reset = 0000h]

Power Management Module Control Register 2

Figure 2-6. PMMCTL2 Register

15	14	13	12	11	10	9	8
Reserved		REFBGRDY	REFGENRDY	BGMODE	Reserved	REFBGACT	REFGENACT
r-0	r-0	r-(0)	r-(0)	r-(0)	r0	r-(0)	r-(0)
7	6	5	4	3	2	1	0
REFBGEN	REFGEN	REFVSEL		TSENSOREN	Reserved	EXTREFEN	INTREFEN
rw-0	rw-0	rw-(0)	rw-(0)	rw-(0)	r0	rw-(0)	rw-(0)

Table 2-4. PMMCTL2 Register Description

Bit	Field	Type	Reset	Description
15-14	Reserved	R	0h	Reserved. Always reads as 0
13	REFBGRDY(1)	R	0h	Buffered bandgap voltage ready status. 0b = Buffered bandgap voltage is not ready to be used 1b = Buffered bandgap voltage is ready to be used
12	REFGENRDY(1)	R	0h	Variable reference voltage ready status. 0b = Reference voltage output is not ready to be used. 1b = Reference voltage output is ready to be used
11	BGMODE	R	0h	Bandgap mode. Ready only. 0b = Static mode (higher precision) 1b = Sampled mode (lower power consumption)
10	Reserved	R	0h	Reserved. Always reads as 0
9	REFBGACT(1)	R	0h	Reference bandgap active. Ready only. 0b = Reference bandgap buffer not active 1b = Reference bandgap buffer active
8	REFGENACT	R	0h	Reference generator active. Read only. 0b = Reference generator not active 1b = Reference generator active
7	REFBGEN	RW	0h	Bandgap and bandgap buffer trigger. If written with a 1, the generation of the buffered bandgap voltage is started. When the bandgap buffer voltage request is set, this bit is cleared by hardware or writing 0. 0b = No trigger 1b = Generation of the bandgap voltage is started by writing 1 or by a hardware trigger
6	REFGEN	RW	0h	Reference generator trigger. If written with a 1, the generation of the variable reference voltage is started. When the reference voltage request is set, this bit is cleared by hardware or writing 0. 0b = No trigger 1b = Generation of the reference voltage is started by writing 1 or by a hardware trigger
5-4	REFVSEL	RW	0h	Internal shared reference voltage level select. 00b = 1.5 V 01b = 2.0 V (Enhanced shared reference systems only) 10b = 2.5 V (Enhanced shared reference systems only) 11b = Reserved
3	TSENSOREN	RW	0h	Temperature sensor enable 0b = Disable temperature sensor 1b = Enable temperature sensor
2	Reserved	R	0h	Reserved. Always reads as 0

(1) This bit resets to logic 0 after reset. It might change to logic 1 shortly after reset when the reference is ready. In 16-MHz systems with only the 1.5-V internal shared reference, PMMCTL2 often reads as 0x3200 after reset, because the reference is ready before user code starts execution. TI recommends checking this bit before using the reference.

Table 2-4. PMMCTL2 Register Description (continued)

Bit	Field	Type	Reset	Description
1	EXTREFEN	RW	0h	External reference output enable 0b = Disable external reference output 1b = Enable internal reference output
0	INTREFEN	RW	0h	Internal reference enable 0b = Disable internal reference 1b = Enable internal reference

2.3.4 PMMIE Register (offset = 0Eh) [reset = 0000h] (External)

Power Management Module Interrupt Enable Register

Figure 2-7. PMMIE Register

15	14	13	12	11	10	9	8
Reserved							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
Reserved							
r-0	r-0	r0	r0	r0	r0	r0	r0

Table 2-5. PMMIE Register Description

Bit	Field	Type	Reset	Description
15-0	Reserved	R	0h	Reserved. Always reads as 0.

2.3.5 PMMIFG Register (offset = 0Ah) [reset = 0000h] (External)

Power Management Module Interrupt Flag Register

Figure 2-8. PMMIFG Register

15	14	13	12	11	10	9	8
PMMLPM5IFG	Reserved	SVSHIFG	Reserved		PMMPORIFG	PMMRSTIFG	PMMBORIFG
rw-{0}	r0	rw-{0}	r-(1)	r-(0)	rw-[0]	rw-{0}	rw-{0}
7	6	5	4	3	2	1	0
Reserved							
r-0	r-0	r0	r0	r0	r0	r0	r0

Table 2-6. PMMIFG Register Description

Bit	Field	Type	Reset	Description
15	PMMLPM5IFG	RW	0h	LPMx.5 flag. This bit has a specific reset conditions. This bit is only set if the system was in LPMx.5 before reset. The bit is cleared by software or by reading the reset vector word. A power failure on the DVCC domain triggered by the high-side SVS (if enabled) or the brownout clears the bit. 0b = Reset not due to wake-up from LPMx.5 1b = Reset due to wake-up from LPMx.5
14	Reserved	R	0h	Reserved. Always reads as 0.
13	SVSHIFG	RW	0h	High-side SVS interrupt flag. This bit has a specific reset conditions. The SVSHIFG interrupt flag is only set if the SVSH is the reset source; that is, DVCC dropped below the high-side SVS levels but remained above the brownout levels. The bit is cleared by software or by reading the reset vector word SYSRSTIV. 0b = Reset not due to SVSH 1b = Reset due to SVSH
12-11	Reserved	R	0h	Reserved. Always reads as 0.
10	PMMPORIFG	RW	0h	PMM software POR interrupt flag. This bit has a specific reset conditions. This interrupt flag is only set if a software POR (PMMSWPOR) is triggered. The bit is cleared by software or by reading the reset vector word. 0b = Reset not due to PMMSWPOR 1b = Reset due to PMMSWPOR
9	PMMRSTIFG	RW	0h	PMM reset pin interrupt flag. This bit has a specific reset conditions. This interrupt flag is only set if the $\overline{\text{RST}}$/NMI pin is the reset source. The bit is cleared by software or by reading the reset vector word. 0b = Reset not due to reset pin 1b = Reset due to reset pin
8	PMMBORIFG	RW	0h	PMM software brownout reset interrupt flag. This bit has a specific reset conditions. This interrupt flag is only set if a software BOR (PMMSWBOR) is triggered. The bit is cleared by software or by reading the reset vector word. 0b = Reset not due to PMMSWBOR 1b = Reset due to PMMSWBOR
7-0	Reserved	R	0h	Reserved. Always reads as 0.

2.3.6 PM5CTL0 Register (offset = 10h) [reset = 0011h]

Power Mode 5 Control Register 0

Figure 2-9. PM5CTL0 Register

15	14	13	12	11	10	9	8
Reserved							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
Reserved		LPM5SM	LPM5SW	Reserved			LOCKLPM5
r0	r0	rw-[0]	rw-[1]	r0	r0	r0	rw-[1]

Table 2-7. PM5CTL0 Register Description

Bit	Field	Type	Reset	Description
15-6	Reserved	R	0h	Reserved. Always reads as 0.
5	LPM5SM	RW	0h	Specifies the operation mode of the LPM3.5 switch. Only available in the FR203x, FR211x, FR2100, FR2000, FR231x, FR2433, FR2422, FR263x, FR253x, FR252x, and FR413x devices. 0b = Automatic mode. The LPM3.5 switch is fully handled by the circuitry during mode switch. 1b = Manual mode. The LPM3.5 switch is specified by LPM5SW bit setting in software.
4	LPM5SW	RW	1h	Reports or sets the LPM3.5 switch connection, based on the switch mode set by LPM5SM. When LPM5SW = 1, the $V_{LPM3.5}$ domain can accept full-speed read and write operation by the CPU MCLK. If the switch is disconnected (LPM5SW = 0), all peripherals within this domain can accept clock operation no faster than 40 kHz. In automatic mode (LPM5SM = 0), this bit represents the switch connection between V_{core} and $V_{LPM3.5}$. Any write to this bit has no effect. In manual mode (LPM5SM = 1), this bit is read/write by software. When this bit is set, the switch connection between V_{core} and $V_{LPM3.5}$ is connected. Otherwise, the switch is disconnected. Only available in the FR203x, FR211x, FR2100, FR2000, FR231x, FR2433, FR2422, FR263x, FR253x, FR252x, and FR413x devices. 0b = LPMx.5 switch disconnected 1b = LPMx.5 switch connected
3-1	Reserved	R	0h	Reserved. Always reads as 0.
0	LOCKLPM5	RW	1h	Lock I/O pin and other LPMx.5 relevant (for example, RTC) configurations upon entry to or exit from LPMx.5. After the LOCKLPM5 bit is set, it can be cleared only by software or by a power cycle. This bit is reset by a power cycle; that is, if SVSH (if enabled) or brownout triggered a reset. 0b = LPMx.5 configuration is not locked and defaults to its reset condition. 1b = LPMx.5 configuration remains locked. Pin state is held during LPMx.5 entry and exit.