# Power Management Module and Supply Voltage Supervisor

This chapter describes the operation of the Power Management Module (PMM) and Supply Voltage Supervisor (SVS).

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## 2.1 Power Management Module (PMM) Introduction

PMM features include:

- Wide supply voltage ($DV_{CC}$) range: 2.0 V to 3.6 V
- Generation of voltage for the device core ($V_{CORE}$)
- Supply voltage supervisor (SVS) for $DV_{CC}$ and $V_{CORE}$
- Brownout reset (BOR)
- Software accessible power-fail indicators
- I/O protection during power-fail condition

The PMM manages all functions related to the power supply and its supervision for the device. Its primary functions are first to generate a supply voltage for the core logic, and second, provide several mechanisms for the supervision of both the voltage applied to the device ($DV_{CC}$) and the voltage generated for the core ($V_{CORE}$).

The PMM uses an integrated low-dropout voltage regulator (LDO) to produce a secondary core voltage ($V_{CORE}$) from the primary one applied to the device ($DV_{CC}$). In general, $V_{CORE}$ supplies the CPU, memories, and the digital modules, while $DV_{CC}$ supplies the I/Os and analog modules. The $V_{CORE}$ output is maintained using a dedicated voltage reference. The input or primary side of the regulator is referred to in this chapter as its high side. The output or secondary side is referred to in this chapter as its low side.

The block diagram of the PMM is shown in Figure 2-1.

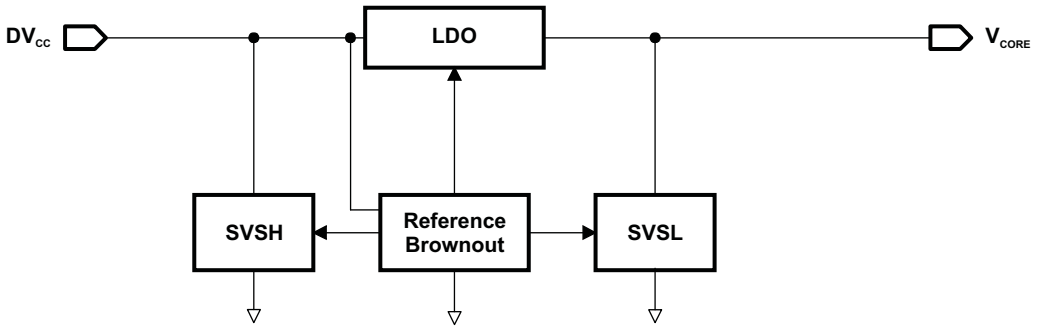


**Figure 2-1. PMM Block Diagram**

## 2.2 PMM Operation

### 2.2.1 $V_{CORE}$ and the Regulator

$DV_{CC}$ can be powered from a wide input voltage range, but the core logic of the device must be kept at a voltage lower than what this range allows. For this reason, a regulator has been integrated into the PMM. The regulator derives the necessary core voltage ($V_{CORE}$) from $DV_{CC}$.

The regulator supports two different load settings to optimize power. The high-performance mode is active when:

- The CPU is in active, LPM0, LPM1, or LPM2 modes
- A clock source greater than 100 kHz is used to drive any module
- An interrupt or DMA transfer is executed
- JTAG is active

Otherwise, the low-power mode is used. The hardware controls the load settings automatically, according to the criteria above.

### 2.2.2 Supply Voltage Supervisor

The high-side supervisor ($SVS_H$) and the low-side supervisor ($SVS_L$) oversee $DV_{CC}$ and $V_{CORE}$, respectively. The high-side supervisor ($SVS_H$) is always active in all power modes. It can be disabled only in LPM4.5 with SVSHE = 0. By default the low-side supervisor ($SVS_L$) is enabled in active mode, LPM0, LPM1, and LPM2. It can be disabled in LPM1 and LPM2 with SVSLE = 0. The $SVS_L$ is always disabled in LPM3, LPM3.5, LPM4, and LPM4.5.

#### 2.2.2.1 SVS Thresholds

As Figure 2-2 shows, there is hysteresis built into the supervision thresholds, such that the thresholds in force depend on whether the voltage rail is going up or down.

The behavior of the SVS according to these thresholds is best portrayed graphically. Figure 2-2 shows how the supervisors respond to various supply failure conditions.

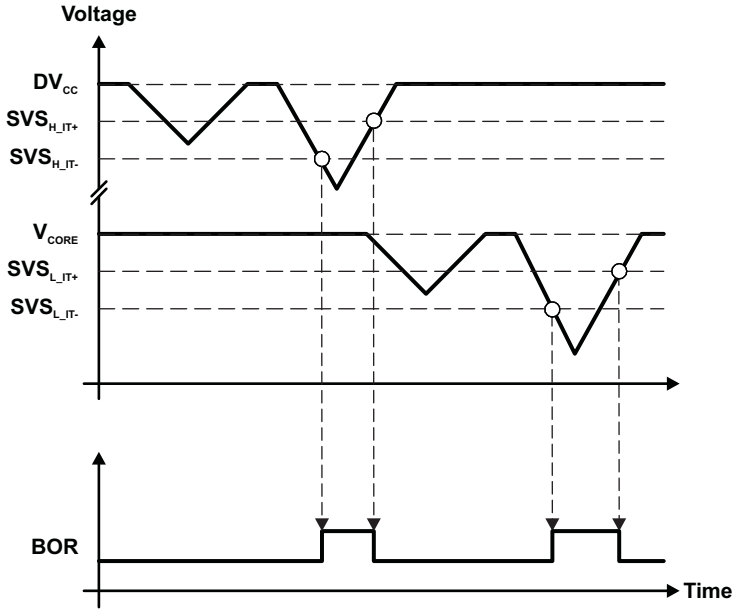


**Figure 2-2. High-Side and Low-Side Voltage Failure and Resulting PMM Actions**

### 2.2.3 Supply Voltage Supervisor - Power-Up

When the device is powering up, the $SVS_H$ and $SVS_L$ functions are enabled by default. Initially, $DV_{CC}$ is low, and therefore the PMM holds the device in BOR reset. When both the $SVS_H$ and $SVS_L$ levels are met, the reset is released. Figure 2-3 shows this process.

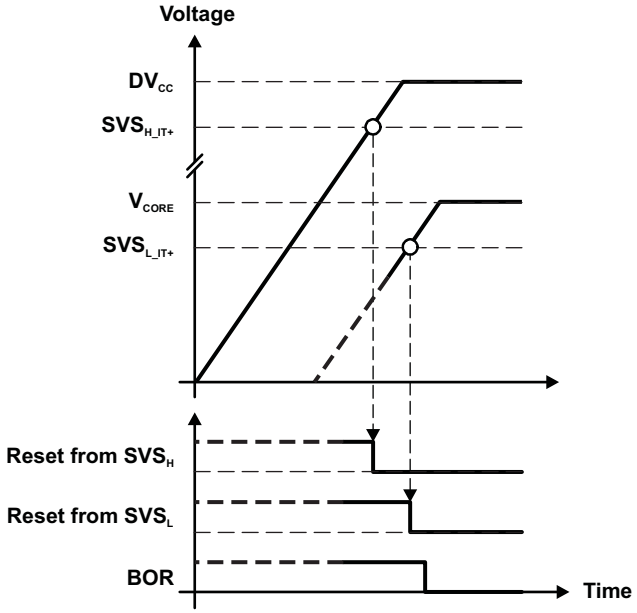


**Figure 2-3. PMM Action at Device Power-Up**

After power-up is complete, both voltage domains are supervised while the respective modules are enabled.

### 2.2.4 LPM3.5, LPM4.5

LPM3.5 and LPM4.5 are additional low-power modes in which the regulator of the PMM is completely disabled, providing additional power savings. Because there is no power supplied to $V_{CORE}$ during LPMx.5, the CPU and all digital modules including RAM are unpowered. This disables the entire device and, as a result, the contents of the registers and RAM are lost. Any essential values should be stored to FRAM prior to entering LPMx.5. See the SYS module for complete descriptions and uses of LPMx.5.

### 2.2.5 Brownout Reset (BOR)

The primary function of the brownout reset (BOR) circuit occurs when the device is powering up. It is functional very early in the power-up ramp, generating a BOR that initializes the system. It also functions when no SVS is enabled and a brownout condition occurs. It sustains this reset until the input power is sufficient for the logic, to enable proper reset of the system.

In an application, it may be desired to cause a BOR via software. Setting PMMSWBOR causes a software-driven BOR. PMMBORIFG is set accordingly. Note that a BOR also initiates a POR and PUC. PMMBORIFG can be cleared by software or by reading SYSRSTIV. Similarly, it is possible to cause a POR via software by setting PMMSWPOR. PMMPORIFG is set accordingly. A POR also initiates a PUC. PMMPORIFG can be cleared by software or by reading SYSRSTIV. Both PMMSWBOR and PMMSWPOR are self clearing. See the SYS module for complete descriptions of BOR, POR, and PUC resets.

### 2.2.6 $\overline{RST}$/NMI

The external $\overline{RST}$/NMI terminal is pulled low on a BOR reset condition. The $\overline{RST}$/NMI can be used as reset source for the rest of the application.

### 2.2.7 PMM Interrupts

Interrupt flags generated by the PMM are routed to the system NMI interrupt vector generator register, SYSSNIV. When the PMM causes a reset, a value is generated in the system reset interrupt vector generator register, SYSRSTIV, corresponding to the source of the reset. These registers are defined within the SYS module. More information on the relationship between the PMM and SYS modules is available in the SYS chapter.

### 2.2.8 Port I/O Control

The PMM provides a means of ensuring that I/O pins cannot behave in uncontrolled fashion during an undervoltage event. During these times, outputs are disabled, both normal drive and the weak pullup or pulldown function. If the CPU is functioning normally, and then an undervoltage event occurs, any pin configured as an input has its PxIN register value locked when the event occurs, until voltage is restored. During the undervoltage event, external voltage changes on the pin are not registered internally. This helps prevent erratic behavior from occurring.

## 2.3 PMM Registers

The PMM registers are listed in Table 2-1. The base address of the PMM module can be found in the device-specific data sheet. The address offset of each PMM register is given in Table 2-1. The password defined in the PMMCTL0 register controls access to all PMM registers except PM5CTL0. PM5CTL0 can be accessed without a password. After the correct password is written, the write access is enabled (this includes byte access to the PMMCTL0 lower byte). The write access is disabled by writing a wrong password in byte mode to the PMMCTL0 upper byte. Word accesses to PMMCTL0 with a wrong password triggers a PUC. A write access to a register other than PMMCTL0 while write access is not enabled causes a PUC.

**NOTE:** All registers have word or byte register access. For a generic register *ANYREG*, the suffix "_L" (*ANYREG_L*) refers to the lower byte of the register (bits 0 through 7). The suffix "_H" (*ANYREG_H*) refers to the upper byte of the register (bits 8 through 15).

**Table 2-1. PMM Registers**

| Offset | Acronym | Register Name | Type | Access | Reset | Section |
|---|---|---|---|---|---|---|
| 00h | PMMCTL0 | PMM control register 0 | Read/write | Word | 9660h | Section 2.3.1 |
| 00h | PMMCTL0_L | | Read/write | Byte | 60h | |
| 01h | PMMCTL0_H | | Read/write | Byte | 96h | |
| 0Ah | PMMIFG | PMM interrupt flag register | Read/write | Word | 0000h | Section 2.3.2 |
| 0Ah | PMMIFG_L | | Read/write | Byte | 00h | |
| 0Bh | PMMIFG_H | | Read/write | Byte | 00h | |
| 10h | PM5CTL0 | Power mode 5 control register 0 | Read/write | Word | 0000h | Section 2.3.3 |
| 10h | PM5CTL0_L | | Read/write | Byte | 00h | |
| 11h | PM5CTL0_H | | Read/write | Byte | 00h | |

### 2.3.1 PMMCTL0 Register

Power Management Module Control Register 0

**Figure 2-4. PMMCTL0 Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| PMMPW | | | | | | | |
| rw-1 | rw-0 | rw-0 | rw-1 | rw-0 | rw-1 | rw-1 | rw-0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | SVSHE | SVSLE | PMMREGOFF | PMMSWPOR | PMMSWBOR | Reserved | Reserved |
| r0 | rw-[1] | rw-[1] | rw-[0] | rw-(0) | rw-[0] | r0 | rw-{0} |

**Table 2-2. PMMCTL0 Register Description**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-8 | PMMPW | RW | 96h | PMM password. Always read as 096h. When using word operations, must be written with 0A5h or a PUC is generated. When using byte operation, writing 0A5h unlocks all PMM registers. When using byte operation, writing anything different than 0A5h locks all PMM registers. |
| 7 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 6 | SVSHE | RW | 1h | High-side SVS enable<br>0b = High-side SVS (SVSH) is disabled in LPM4.5. SVSH is always enabled in active mode and LPM0, LPM1, LPM2, LPM3, LPM4, and LPM3.5.<br>1b = SVSH is always enabled. |
| 5 | SVSLE | RW | 1h | Low-side SVS enable<br>0b = Low-side SVS (SVSL) is disabled in low-power modes. SVSL is always enabled in active mode and LPM0.<br>1b = SVSL is enabled in LPM0, LPM1, and LPM2. SVSL is always enabled in AM and always disabled in LPM3, LPM4, LPM3.5, and LPM4.5. |
| 4 | PMMREGOFF | RW | 0h | Regulator off<br>0b = Regulator remains on when going into LPM3 or LPM4<br>1b = Regulator is turned off when going to LPM3 or LPM4. System enters LPM3.5 or LPM4.5, respectively. |
| 3 | PMMSWPOR | RW | 0h | Software POR. Setting this bit to 1 triggers a POR. This bit is self clearing. |
| 2 | PMMSWBOR | RW | 0h | Software brownout reset. Setting this bit to 1 triggers a BOR. This bit is self clearing. |
| 1 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 0 | Reserved | RW | 0h | Reserved. Must always be written as 0. |

### 2.3.2 PMMIFG Register

Power Management Module Interrupt Flag Register

**Figure 2-5. PMMIFG Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| PMMLPM5IFG | Reserved | SVSHIFG | SVSLIFG | Reserved | PMMPORIFG | PMMRSTIFG | PMMBORIFG |
| rw-{0}(1) | r0 | rw-{0}(1) | rw-{0}(1) | r0 | rw-[0](1) | rw-{0}(1) | rw-{0}(1) |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | | | |
| r0 | r0 | r0 | r0 | r0 | r0 | r0 | r0 |

(1) This bit indicates a specific reset condition. See bit description concerning reset conditions.

**Table 2-3. PMMIFG Register Description**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15 | PMMLPM5IFG | RW | 0h | LPMx.5 flag. This bit is only set if the system was in LPMx.5 before. The bit is cleared by software or by reading the reset vector word. A power failure on the DVCC domain triggered by the high-side SVS (if enabled) or the brownout clears the bit.<br>0b = Reset not due to wake-up from LPMx.5<br>1b = Reset due to wake-up from LPMx.5 |
| 14 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 13 | SVSHIFG | RW | 0h | High-side SVS interrupt flag. This interrupt flag is only set if the SVSH is the reset source; that is, if DVCC dropped below the high-side SVS levels but remained above the brownout levels. The bit is cleared by software or by reading the reset vector word.<br>0b = Reset not due to SVSH<br>1b = Reset due to SVSH |
| 12 | SVSLIFG | RW | 0h | Low-side SVS interrupt flag. This interrupt flag is only set if the SVSL is the reset source; that is if the core voltage dropped below the low-side SVS levels but DVCC remained above the SVSH levels. The bit is cleared by software or by reading the reset vector word.<br>0b = Reset not due to SVSL<br>1b = Reset due to SVSL |
| 11 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 10 | PMMPORIFG | RW | 0h | PMM software POR interrupt flag. This interrupt flag is only set if a software POR (PMMSWPOR) is triggered. The bit is cleared by software or by reading the reset vector word.<br>0b = Reset not due to SWPOR<br>1b = Reset due to SWPOR |
| 9 | PMMRSTIFG | RW | 0h | PMM reset pin interrupt flag. This interrupt flag is only set if the RST/NMI pin is the reset source. The bit is cleared by software or by reading the reset vector word.<br>0b = Reset not due to reset pin<br>1b = Reset due to reset pin |
| 8 | PMMBORIFG | RW | 0h | PMM software brownout reset interrupt flag. This interrupt flag is only set if a software BOR (PMMSWBOR) is triggered. The bit is cleared by software or by reading the reset vector word.<br>0b = Reset not due to SWBOR<br>1b = Reset due to SWBOR |
| 7-0 | Reserved | R | 0h | Reserved. Always reads as 0. |

### 2.3.3 PM5CTL0 Register

Power Mode 5 Control Register 0

**Figure 2-6. PM5CTL0 Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | |
| r0 | r0 | r0 | r0 | r0 | r0 | r0 | r0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | | | LOCKLPM5 |
| r0 | r0 | r0 | r0 | r0 | r0 | r0 | rw-{0}(1) |

(1) This bit is reset by a power cycle; that is, if SVSH (if enabled) or brownout triggers a reset.

**Table 2-4. PM5CTL0 Register Description**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-1 | Reserved | R | 0h | Reserved. Always reads as 0. |
| 0 | LOCKLPM5 | RW | 0h | Lock I/O pin and other LPMx.5 relevant (for example, RTC) configurations upon entry to or exit from LPMx.5. When power is applied to the device and this bit is set, the bit can only be cleared by the user or by another power cycle.<br>0b = LPMx.5 configuration is not locked and defaults to its reset condition.<br>1b = LPMx.5 configuration remains locked. Pin state is held during LPMx.5 entry and exit. |