Chapter 3

Power Management Module (PMM)

The Power Management Module (PMM) manages all functions related to the power supply and its supervision for the device. This chapter describes the PMM.

3.1 Power Management Module Introduction

PMM features include:

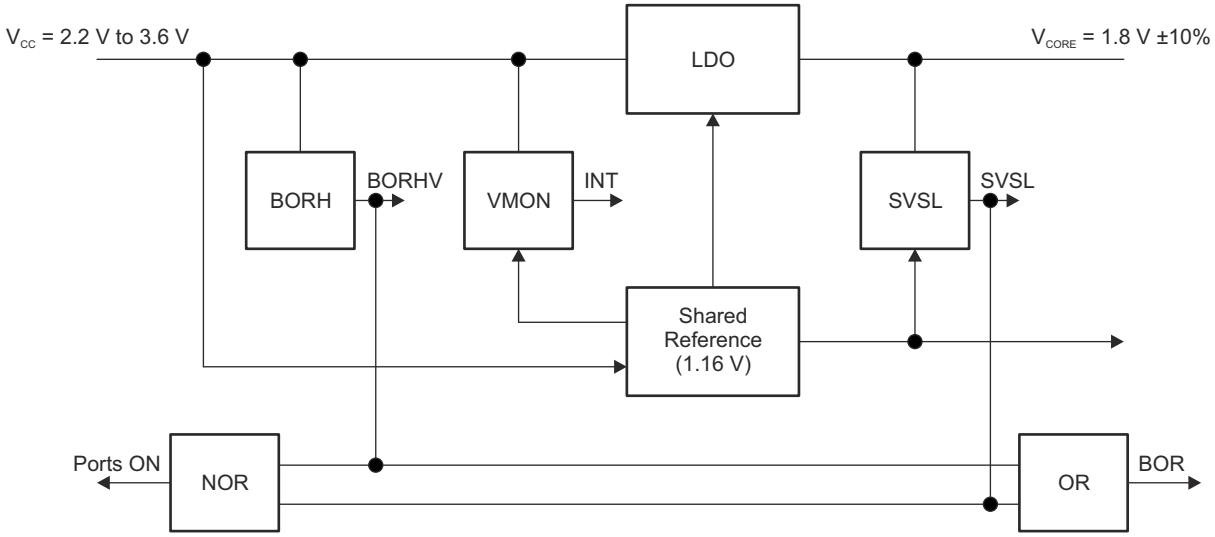
- Supply voltage (V_{CC}) range: 2.2 V to 3.6 V
- High-side brownout reset (BORH)
- Supply voltage monitor (VMON) for V_{CC} with programmable threshold levels and monitoring of external pin (VMONIN) against internal reference
- Generation of fixed voltage of 1.8 V for the device core (V_{CORE})
- Supply voltage supervisor (SVS) for V_{CORE}
- Precise 1.16-V reference for the entire device and integrated temperature sensor.

The PMM manages all functions related to the power supply and its supervision for the device. Its primary functions are:

1. To generate a supply voltage for the core logic
2. To provide mechanisms for the supervising and monitoring of both the voltage applied to the device (V_{CC}) and the voltage generated for the core (V_{CORE})

The PMM uses an integrated low-dropout voltage regulator (LDO) to produce a secondary core voltage (V_{CORE}) from the primary voltage applied to the device (V_{CC}). V_{CORE} supplies the CPU, memories (flash and RAM), and the digital modules, while V_{CC} supplies the I/Os and analog modules. The V_{CORE} output is maintained using a voltage reference that is generated by the reference block within the PMM. The input or primary side of the regulator is referred to in this chapter as its high side. The output or secondary side is referred to in this chapter as its low side.

Figure 3-1 shows the block diagram of the power management system.



A. BORHV is active-high polarity (1 = V_{CC} domain is in reset). SVSL is active-high polarity (1 = V_{CORE} domain is in reset).

Figure 3-1. PMM and REF Block Diagram

3.2 Power Management Module Operation

3.2.1 Voltage Regulator

V_{CC} can be powered from a wide input voltage range, but the core logic of the device must be kept at a voltage lower than what this range allows. For this reason, a regulator has been integrated into the PMM. The regulator derives the necessary core voltage (V_{CORE}) from V_{CC}.

3.2.2 Brownout Reset (BOR) and Supply Voltage Supervisor (SVS) – Power Up

The primary function of the brownout reset (BOR) circuit occurs when the device is powering up. It is functional very early in the power-up ramp, generating a reset that initializes the system. It also functions when a brownout condition occurs after power-up. It sustains this reset until the input voltage is high enough for a proper reset of the system.

There is a supply voltage supervisor (SVSL) on the low side of the PMM, which gives an indication that the V_{CORE} is in the usable range for the digital core and the rest of the circuitry powered on the core voltage. Early in the power-up ramp, V_{CC} is low and, therefore, the PMM holds the device in BOR reset. After V_{CC} crosses the brownout level, the LDO is turned ON, and starts to ramp up V_{CORE}. When V_{CORE} rises above the SVSL level, the BOR reset is released after a small delay. Figure 3-2 shows this process.

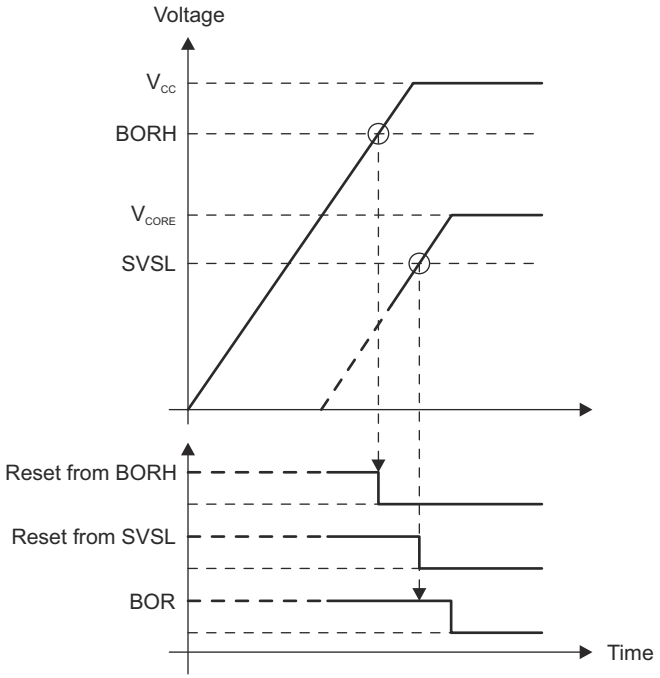


Figure 3-2. Power-Up Sequence

3.2.3 Voltage Monitor (VMON)

The voltage monitor (VMON) compares the voltage applied on either the external device pin VMONIN or the on-chip DVCC to a specified limit. If the monitored voltage falls below the trip level, VMON triggers an interrupt.

The voltage monitor is disabled after power up. The application must enable this module by programming appropriate values into the VMONLVLx bits in the VMONCTL register:

- Set VMONLVLx = 001b, 010b, or 011b to monitor DVCC against one of the three user-selectable voltage trip levels. See Section 3.3.2 for details on programmable voltage trip levels for monitoring DVCC.
- Set VMONLVLx = 111b to monitor the voltage on the VMONIN pin against an internal reference voltage.

The interrupt flag (VMONIFG) and interrupt enable (VMONIE) are defined in VMONCTL register. When VMONIFG is set and VMONIE is enabled, the voltage monitor triggers a maskable interrupt to the CPU. VMONIFG flag indicates the status of supply being monitored. When VMON is disabled, VMONIFG is 0.

Software can write into VMONIFG to emulate a VMON interrupt when the module is disabled. When VMON is enabled, software writes to VMONIFG are ignored, and VMONIFG reflects the status of the supply being monitored.

VMON requires a settling time of 0.5 µs (typical) when it is turned on or when the monitoring mode is changed from VMONIN to DVCC or from DVCC to VMONIN. VMONIFG is not reliable during this settling time. There is no settling time involved when the DVCC monitoring trip level is changed from one value to another, and VMONIFG status is always reliable.

In the DVCC monitoring mode, VMONIFG = 0 when the DVCC is above the selected voltage trip level, and VMONIFG = 1 when DVCC is below the selected voltage trip level.

In the external voltage monitoring mode, VMONIFG = 0 when the voltage applied on the VMONIN pin is above the internal reference voltage, and VMONIFG = 1 when the voltage on the VMONIN pin is below the internal reference voltage. In this mode, it is recommended to use an external voltage divider with its input connected to an external voltage and its output connected to the VMONIN pin (see Figure 3-3).

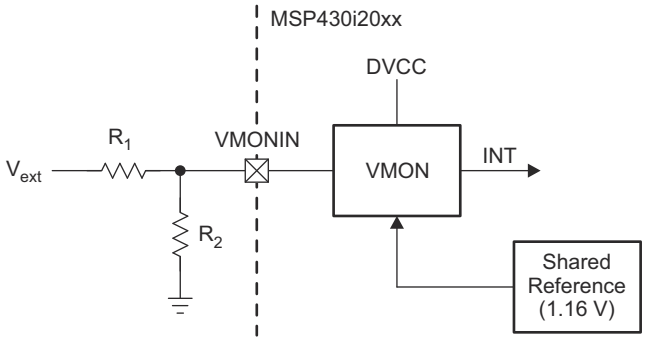


Figure 3-3. VMONIN Recommended External Circuitry

Compared to the DVCC monitoring mode, one advantage of the external voltage monitoring mode is that the voltage divider allows voltages higher than DVCC to be monitored without exceeding the absolute maximum ratings defined in the device-specific datasheet. However, the voltage applied on VMONIN should only be applied after powering up the device. Another advantage of this mode is that DVCC can be monitored externally at higher trip levels than the programmable trip levels. This can allow more time for completing tasks before losing power.

When using external voltage monitoring mode, the external voltage divider must be sized accordingly. Choose a desired voltage trip level (for example, 4.8 V) for V_{ext} and a resistance (for example, 10 kΩ) for R2. Calculate the resistance for R1 using Equation 1 where the VMONIN trip-level voltage is defined in the device-specific data sheet, and then select the nearest standard resistor value for R1.

$$R_1 = R_2 \times \left(\frac{V_{ext}}{VMONIN_{trip\ level}} - 1 \right) \quad (1)$$

When the voltage monitor is enabled and VMONIFG = 1, software cannot clear the flag as long as the low-voltage condition persists. The voltage monitor is disabled and VMONIFG is cleared by hardware when the VMONLVLx bits are programmed to 000b or with any of the reserved values. When the voltage monitor is disabled and an interrupt is triggered from software by writing 1 to VMONIFG and VMONIE bits, the VMONIFG bit is cleared when the CPU enters the VMON interrupt service routine.

3.2.3.1 Voltage Monitor Timing Waveforms

The following waveforms show the operation of VMON in different use cases.

Use Case 1: VMON is configured to monitor DVCC or VMONIN and low voltage is detected.

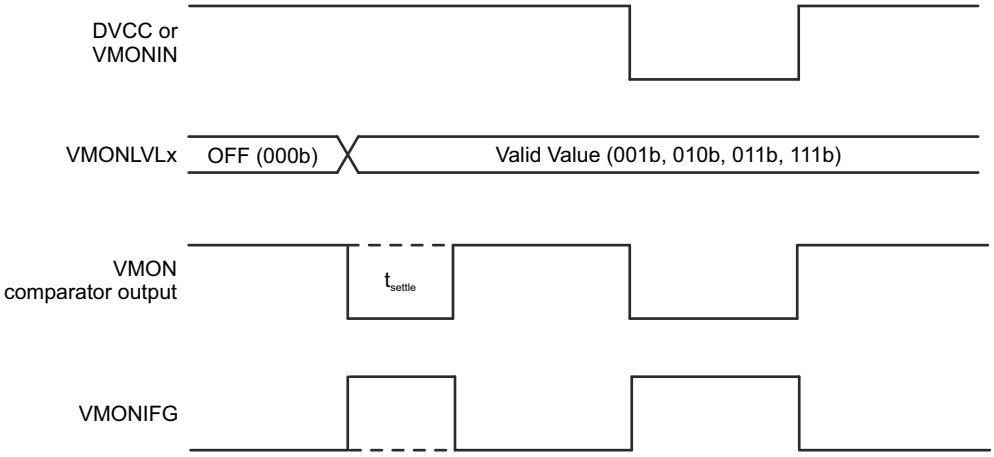


Figure 3-4. Voltage Monitor Timing, Use Case 1

Use Case 2: VMON is configured to monitor DVCC or VMONIN and low voltage is detected –> VMON disabled by software.

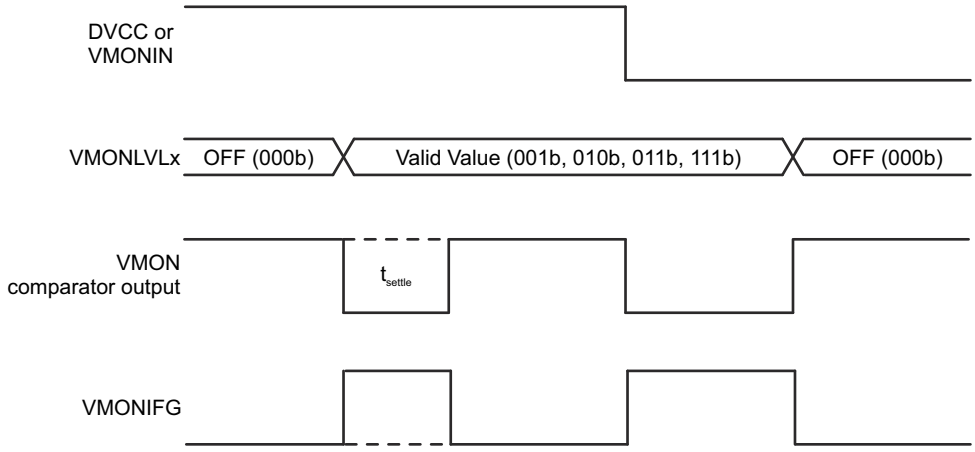


Figure 3-5. Voltage Monitor Timing, Use Case 2

Use Case 3: VMON is configured to monitor VMONIN and low voltage is detected –> VMON is switched to monitor DVCC and low voltage is detected –> VMON disabled by software during low voltage condition.

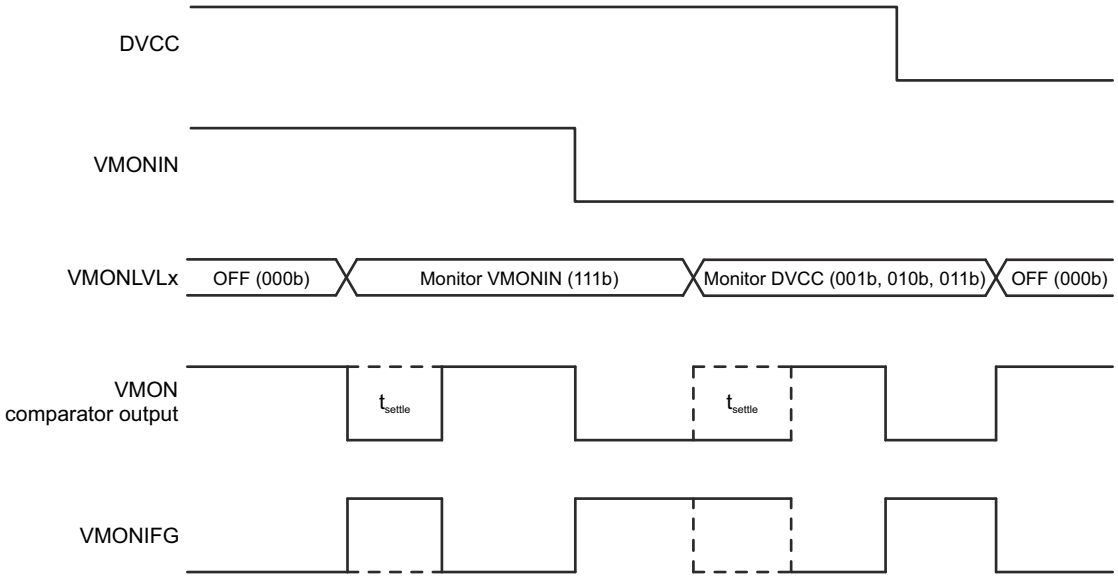


Figure 3-6. Voltage Monitor Timing, Use Case 3

3.2.4 LPM4.5

LPM4.5 is an additional low-power mode in which the regulator of the PMM is disabled to provide additional power savings. Because there is no power supplied to V_{CORE} during LPM4.5, the CPU and all digital modules including RAM are unpowered. This disables nearly the entire device, and the contents of the registers and RAM are lost. Any essential values should be stored to flash prior to entering LPM4.5. LPM4.5 mode is entered when REGOFF bit is set to 1 in the LPM45CTL register followed by LPM4 programming in the CPU status register.

Because the regulator of the PMM is disabled upon entering LPM4.5, all I/O register configurations are lost. Therefore, the configuration of I/O pins must be handled differently to ensure that all pins in the application behave in a controlled manner upon entering and exiting LPM4.5. Properly setting the I/O pins is critical to achieving the lowest possible power consumption in LPM4.5, as well as preventing any possible uncontrolled input or output I/O state in the application. The application has complete control of the I/O pin conditions that prevent unwanted spurious activity upon entry and exit from LPM4.5. The I/O pin state is held and locked based on the settings prior to LPM4.5 entry. Upon entry into LPM4.5, the LOCKLPM45 bit in the LPM45CTL register of the PMM module is set automatically. Note that only the pin condition is retained. All other port configuration register settings are lost.

Exit from LPM4.5 is possible with an active-low event on $\overline{\text{RST}}$/NMI pin, a power-on cycle, or by specific I/O. Refer to device-specific data sheet for details on LPM4.5 wakeup capable I/Os. Any exit from LPM4.5 causes a BOR. Program execution continues at the location stored in the system reset vector location 0FFFEh. The LPM45IFG bit inside the PMM module is set to indicate that the device was in LPM4.5 prior to the wakeup event. During LPM4.5, all I/O pin conditions are automatically locked to the current state. Upon exit from LPM4.5, the I/O pin conditions remain locked until the application unlocks them by writing 0 to the LOCKLPM45 bit. See Section 6.3 for complete details.

3.2.5 Shared Reference

The REF module is a general-purpose reference system that generates voltage references required for other subsystems such as digital-to-analog converters, analog-to-digital converters, and comparators.

Features of the REF include:

- Centralized bandgap with excellent PSRR, temperature coefficient, and accuracy
- Unbuffered bandgap voltage available to rest of system
- Integrated temperature sensor

Figure 3-7 shows the block diagram of the REF module.

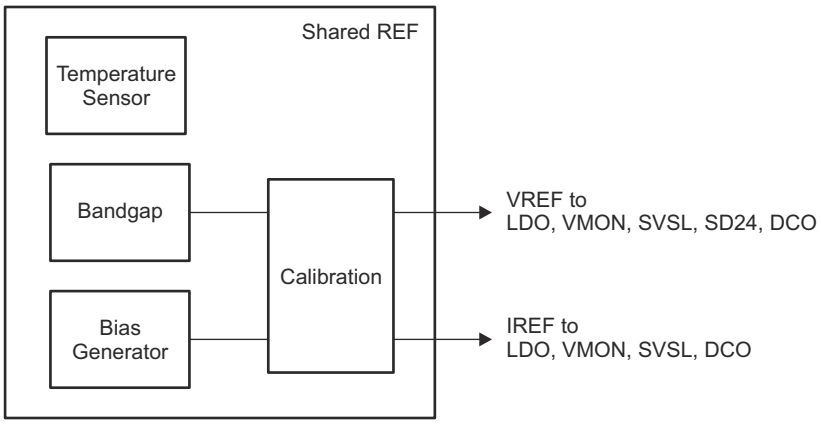


Figure 3-7. REF Block Diagram

The REF module provides all of the necessary voltage references for use by various peripheral modules throughout the system. These include, but are not limited to, devices that contain an LDO, VMON, SVSL, SD24, analog-to-digital converter (ADC), digital-to-analog converter (DAC), or digitally controlled oscillator (DCO).

The REF subsystem contains a high-performance bandgap. This bandgap has good accuracy, low temperature coefficient, and high PSRR while operating at low power. Additionally, the REF generates bias currents required for the LDO, VMON, SVSL, and DCO.

3.2.5.1 Reference Calibration

The application should calibrate the reference voltage and current for the specified accuracy by programming the REFCAL0 and REFCAL1 registers. The calibration values are stored in the flash information memory in TLV format. See the REF section in the device-specific data sheet for complete the electrical specification of the REF module.

3.2.5.2 Temperature Sensor

The REF subsystem also includes the temperature sensor circuitry, which is derived from the bandgap. The temperature sensor is used by a sigma-delta ADC (SD24) to measure a voltage proportional to temperature. The temperature sensor is not enabled by default, and it is active only when the sigma-delta ADC selects the temperature sensor as an input.

3.3 PMM Registers

Table 3-1 lists the PMM registers.

Table 3-1. PMM Registers

Address	Acronym	Register Name	Type	Access	Reset	Section
0060h	LPM45CTL	LPM4.5 Control	Read/Write	Byte	00h	Section 3.3.1
0061h	VMONCTL	Voltage Monitor Control	Read/Write	Byte	00h	Section 3.3.2
0062h	REFCAL0	Reference Calibration 0	Read/Write	Byte	00h	Section 3.3.3
0063h	REFCAL1	Reference Calibration 1	Read/Write	Byte	00h	Section 3.3.4

3.3.1 LPM45CTL Register (address = 0060h) [reset = 00h]

LPM4.5 Control Register

Figure 3-8. LPM45CTL Register

7	6	5	4	3	2	1	0
Reserved			REGOFF	Reserved		LPM45IFG	LOCKLPM45
r0	r0	r0	rw-0	r0	r0	rw-[0]	rw-[0]

Table 3-2. LPM45CTL Register Description

Bit	Field	Type	Reset	Description
7-5	Reserved	R	0h	Reserved. Always reads as 0.
4	REGOFF	RW	0h	PMM regulator off. If this bit is set followed by LPM4 programming, internal voltage regulator is turned off. 0b = PMM voltage regulator is operating 1b = PMM voltage regulator is turned off when LPM4 mode is programmed subsequently
3-2	Reserved	R	0h	Reserved. Always reads as 0.
1	LPM45IFG	RW	0h	LPM4.5 interrupt flag. This bit is set if the system was in LPM4.5 mode before. This bit is cleared by software or by a BOR. 0b = Device was not in LPM4.5 mode 1b = Device was in LPM4.5 mode
0	LOCKLPM45	RW	0h	Lock I/O pin configuration upon entry to or exit from LPM4.5. This bit can only be written as 0. When power is applied to the device, this bit, once set by hardware, can be cleared only by user software or by BOR. 0b = I/O pin configuration is not locked and defaults to its reset condition. 1b = I/O pin configuration remains locked. Pin state is held during LPM4.5 entry and exit.

3.3.2 VMONCTL Register (address = 0061h) [reset = 00h]

Voltage Monitor Control Register

Figure 3-9. VMONCTL Register

7	6	5	4	3	2	1	0
Reserved		VMONIFG	VMONIE	Reserved	VMONLVLx		
r0	r0	rw-(0)	rw-0	r0	rw-(0)	rw-(0)	rw-(0)

Table 3-3. VMONCTL Register Description

Bit	Field	Type	Reset	Description
7-6	Reserved	R	0h	Reserved. Always reads as 0.
5	VMONIFG	RW	0h	VMON interrupt flag 0b = No low-voltage condition 1b = DVCC below the selected threshold or external VMONIN below 1.16 V
4	VMONIE	RW	0h	VMON interrupt enable. If this bit it set, when DVCC or external VMONIN goes below the monitored level, an interrupt is generated
3	Reserved	R	0h	Reserved. Always reads as 0.
2-0	VMONLVLx	RW	0h	Voltage monitor level selection. These bits are used to select between DVCC and external VMONIN pin for voltage monitoring and also to define the monitoring levels when DVCC is being monitored. 000b = Disable VMON 001b = Compare DVCC to 2.35 V (typ) 010b = Compare DVCC to 2.65 V (typ) 011b = Compare DVCC to 2.85 V (typ) 100b = Reserved 101b = Reserved 110b = Reserved 111b = Compare VMONIN to 1.16 V (typ)

3.3.3 REFCAL0 Register (address = 0062h) [reset = 00h]

Reference Calibration 0 Register

Figure 3-10. REFCAL0 Register

7	6	5	4	3	2	1	0
Reserved		BGCOARSE		BGFINE			
r0	r0	rw-[0]	rw-[0]	rw-[0]	rw-[0]	rw-[0]	rw-[0]

Table 3-4. REFCAL0 Register Description

Bit	Field	Type	Reset	Description
7-6	Reserved	R	0h	Reserved. Always reads as 0.
5-4	BGCOARSE	RW	0h	Bandgap voltage coarse calibration.
3-0	BGFINE	RW	0h	Bandgap voltage fine calibration.

3.3.4 REFCAL1 Register (address = 0063h) [reset = 00h]

Reference Calibration 1 Register

Figure 3-11. REFCAL1 Register

7	6	5	4	3	2	1	0
BIASCURRENT				BGCURVE			
rw-[0]	rw-[0]	rw-[0]	rw-[0]	rw-[0]	rw-[0]	rw-[0]	rw-[0]

Table 3-5. REFCAL1 Register Description

Bit	Field	Type	Reset	Description
7-4	BIASCURRENT	RW	0h	Bandgap bias current calibration.
3-0	BGCURVE	RW	0h	Bandgap curvature compensation.